UQAC
Université du Québec
à Chicoutimi

CONCEPTION D'UN CONVERTISSEUR ANALOGIQUE-NUMÉRIQUE À HAUTE PRÉCISION ET BASSE CONSOMMATION DE PUISSANCE AVEC LA TECHNOLOGIE CMOS 65 NM

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MÉMOIRE PRÉSENTÉ À L'UNIVERSITÉ DU QUÉBEC À CHICOUTIMI EN VUE DE L'OBTENTION DU GRADE DE MAÎTRISE ÈS SCIENCES APPLIQUÉES (M. SC. A.) EN INGÉNIERIE

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RÉSUMÉ

Ce mémoire propose une nouvelle architecture d'ADC ΔΣ conçue pour répondre à des exigences strictes en matière de rapport signal sur bruit (SNR) sur une bande passante de plusieurs centaines de kilohertz. L'architecture repose sur la topologie sturdy MASH, dans laquelle le second étage est remplacé par un SAR à filtrage de bruit (NS-SAR). Grâce à la propriété de feedforward intrinsèque au NS-SAR, cette nouvelle topologie permet d'annuler efficacement le bruit de quantification du premier étage.

Le NS-SAR bénéficie aussi de contraintes de conception grandement simplifiées grâce à une amplitude d'entrée réduite et grâce au filtrage additionnel fourni par le premier étage, ce qui atténue les non-idéalités du circuit. Ces caractéristiques permettent une implémentation du NS-SAR à très faible consommation de puissance.

Au niveau circuit, un amplificateur dynamique innovant est proposé pour optimiser le compromis entre la consommation de puissance, l'encombrement et la capacité d'attaquer de grandes charges dans le premier intégrateur du circuit. D'autres techniques de conception contribuent également à maximiser l'efficacité du circuit comme l'utilisation d'un sommateur passif réutilisant les condensateurs du DAC du quantificateur SAR, éliminant ainsi le besoin d'un amplificateur dédié.

L'ADC a été implémenté avec la technologie CMOS 65 nm sur Cadence Virtuoso. Les résultats de simulations démontrent d'excellentes performances comparables à l'état de l'art des ADC à suréchantillonnage. Les spécifications atteintes sont un ratio signal sur bruit et distorsion de 90.3 dB, une bande passante de 500 kHz et une consommation de puissance de 1.633 mW, ce qui correspond à une FOM_{Sc} de 175.2 dB.

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ADC	Analog-to-Digital Converter
BW	Bandwidth
CCIA	Capacitively Coupled Instrumentation Amplifier
CCO	Current-Controlled Oscillator
CDAC	Capacitive DAC
CEF	Cost Effectiveness Factor
CIFF	Cascade of Integrators with Feedforward
CMFB	Common-Mode Feedback
CMOS	Complementary Metal Oxide Semiconductor
CT	Continuous Time
DA	Dynamic Amplifier
DAC	Digital-to-Analog Converter
DR	Dynamic Range
DT	Discrete Time
DWA	Data Weight Averaging
EF	Error Feedback
ENOB	Effective Number of Bits
FFT	Fast Fourrier Transform
FIA	Floating Inverter Amplifier
FIR	Finite Impulse Response
FOM	Figure Of Merit
FOM_{Sc}	Schreier's FOM
FOM_{Wa}	Walden's FOM
HDL	Hardware Description Language
IA	Intelligence Artificielle
IIR	Infinite Impulse Response
IoT	Internet-of-Things
ISG	Interstage Gain
ISI	Intersymbol Interference
LNC-SMASH	Lean Noise-Canceling SMASH
LUT	Lookup Table
MASH	Multi-Stage Noise Shaping
MES	Mismatch Error Shaping
NC-SMASH	Noise-Canceling SMASH

NS-SAR	Noise-Shaping SAR
NTF	Noise Transfer Function
OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier
PLL	Phase-Locked Loop
PSD	Power Spectrum Density
PVT	Process, Voltage and Temperature
PWM	Pulse-Width Modulation
RFC	Recycling Folded Cascode
SAR	Successive Approximation Register
SC	Switched Capacitors
SFDR	Spurious-Free Dynamic Range
S/H	Sample and Hold
SMASH	Sturdy MASH
SNDR	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
SoC	System-on-Chip
SQNR	Signal-to-Quantization-Noise Ratio
STF	Signal Transfer Function
TD	Time Domain
VCDL	Voltage-Controlled Delay Line
VCO	Voltage-Controlled Oscillator
WSN	Wireless Sensor Network

REMERCIEMENTS

Je tiens avant tout à remercier mes directeurs de recherche prof. Alexandre Robichaud et prof. Paul-Vahé Cicek. En plus de prendre le temps de suivre l'évolution de mon projet avec attention et de fournir de précieux conseils et encouragements, ils ont aussi été d'excellents guides dans ma carrière de jeune chercheur. Travailler avec eux est à la fois enrichissant, instructif, motivant et même amusant. J'ai déjà hâte de poursuivre l'aventure au doctorat.

J'aimerais aussi remercier mes parents. Ma mère qui m'a toujours encouragé et motivé de manière indéfectible. Mon père pour son support, ses encouragements et les soupers du samedi pendant lesquels il s'est probablement tapé le contenu en entier de ce mémoire une semaine à la fois.

Finalement, je remercie le CRSNG et le FRQNT pour l'appui financier, ainsi que CMC Microsystems pour l'accès aux outils de conception et aux technologies de fabrication CMOS.

AVANT-PROPOS

Le présent travail de recherche est structuré sous forme d'un mémoire par articles. Chaque chapitre du mémoire correspond à un article ou un acte de conférence publié dans le cadre du projet de recherche.

Le premier chapitre présente une revue de littérature couvrant l'ensemble des architectures de convertisseurs analogiques-numériques à suréchantillonnage.

Le second chapitre couvre la principale innovation du projet de recherche, soit l'élaboration de la nouvelle architecture d'ADC $\Delta\Sigma$ à un haut niveau d'abstraction. Le principe de l'annulation de bruit reposant sur la propriété de feedforward intrinsèque au NS-SAR est introduit avec des simulations haut niveau démontrant le fonctionnement de l'innovation.

Le chapitre suivant constitue le point de départ de la conception du circuit électronique implémentant la nouvelle architecture d'ADC. Ce chapitre se concentre sur le premier intégrateur du circuit. Il s'agit du bloc de circuit ayant les contraintes de conception les plus sévères en raison du bruit thermique. Ainsi, un nouvel amplificateur dynamique hybride permettant d'optimiser l'opération statique et dynamique pour limiter la consommation de puissance est proposé.

L'implémentation du reste du circuit électronique de l'ADC est présentée dans le chapitre quatre. Le circuit de l'ADC $\Delta\Sigma$ complet y est détaillé avec des simulations niveau transistor montrant les performances atteintes.

Le cinquième et dernier chapitre ne provient pas d'un article publié et inclut les derniers résultats de simulation présentant la robustesse du circuit aux variations de procédé, de température et de tension d'alimentation. Les performances de l'ADC conçu dans ce projet de recherche sont aussi comparées à celles de l'état de l'art dans ce chapitre.

INTRODUCTION

PROBLÉMATIQUE DE RECHERCHE

Grâce aux avancées fulgurantes de la microélectronique au cours des dernières décennies, on assiste à un déploiement massif des technologies embarquées, notamment avec l'intelligence artificielle (IA) en périphérie, l'Internet des objets (IoT) et les réseaux de capteurs [1, 2, 3]. Les exigences technologiques actuelles sont particulièrement élevées : les systèmes doivent être toujours plus rapides, plus performants, plus compacts, et surtout plus économiques. Par ailleurs, les circuits doivent être très économes en puissance pour préserver la durée de vie des batteries. Dans ce contexte, les spécifications attendues pour les circuits électroniques explosent, portées par une demande croissante pour des produits de haute technologie.

Le rétrécissement constant des noeuds de fabrication des dés de silicium permet d'améliorer les performances des circuits numériques années après année [4]. Par contre, les circuits analogiques peinent à suivre la cadence puisqu'ils bénéficient beaucoup moins des avantages inhérents aux nouvelles technologies [5]. Les nouveaux noeuds *deep submicron* permettent notamment de réduire l'encombrement des circuits, d'augmenter la fréquence de commutation des transistors numériques et de limiter la consommation de puissance grâce à une réduction des capacités parasites et de la tension d'alimentation. Or, bien que les circuits analogiques puissent bénéficier d'une part de la réduction d'espace et des capacités parasites, il est souvent nécessaire d'augmenter la taille des transistors bien au-delà du minimum technologique pour atteindre des transconductances, des résistances de sortie, et un matching conformes aux spécifications. Aussi, la diminution des tensions d'alimentation limite la plage de tension disponible dans les circuits analogiques, ce qui complique l'empilement des transistors, réduit

la marge de fonctionnement pour maintenir les transistors en saturation et limite l'amplitude maximale des signaux, les rendant plus sensibles au bruit [5].

Ainsi, d'une part, les spécifications explosent, et d'autre part, les nouvelles technologies de fabrication offrent peu d'avantages, voire nuisent aux performances des circuits analogiques. Il n'est donc pas surprenant que la majorité du traitement du signal soit aujourd'hui entièrement réalisé de manière numérique [6]. Cela renforce d'autant plus l'importance des ADC, car de nombreux blocs fonctionnels, historiquement implémentés en électronique analogique, sont désormais réalisés à l'aide de microprocesseurs ou de circuits numériques dédiés. Dans ces architectures, l'ADC devient souvent le seul et dernier maillon analogique du système [5, 6]. L'évolution des techniques et des architectures d'ADC est donc cruciale pour permettre aux circuits modernes d'atteindre les performances attendues. En l'absence de solutions architecturales adaptées, les ADC deviennent rapidement le facteur limitant des systèmes électroniques, tant en termes de consommation de puissance que de précision et de bande passante. Cette tendance ne fera que s'accentuer avec la poursuite du développement des technologies CMOS, qui favorisent toujours davantage les implémentations purement numériques.

Un des cas critiques de cette problématique concerne les applications nécessitant une haute précision, c'est-à-dire un rapport signal sur bruit et distorsion (SNDR) élevé. Dans les ADC, l'augmentation de la précision passe par l'augmentation du nombre de bits, ce qui complexifie les circuits électroniques. Aussi, les contraintes de bruit thermique doivent être resserrées, forçant l'utilisation de grands condensateurs d'échantillonnage. Ces deux facteurs contribuent à une augmentation significative de la consommation de puissance et à une réduction de la bande passante, dégradant ainsi les performances globales de l'ADC.

Dans l'état de l'art, parmi les différentes topologies d'ADC, l'architecture $\Delta\Sigma$ est le choix privilégié pour les applications à haute précision. En effet, le filtrage du bruit de quanti-

fication et le suréchantillonnage caractéristiques de cette topologie permettent de relâcher les contraintes de conception des circuits analogiques, tout en atténuant les exigences liées au bruit thermique [7]. Ainsi, les efforts de ce projet de recherche se concentreront l'amélioration des architectures et des circuits des ADC à suréchantillonnage afin de répondre aux spécifications particulièrement exigeantes des applications émergentes. On vise également de permettre aux interfaces analogiques de suivre le rythme rapide des progrès en électronique numérique, tout en atténuant l'impact limitant des ADC sur les performances globales des circuits intégrés modernes.

OBJECTIFS

Le projet de recherche est défini par un objectif principal se déclinant en plusieurs objectifs secondaires. L'objectif principal du projet de recherche est de développer une nouvelle architecture d'ADC $\Delta\Sigma$ permettant d'atteindre les hautes performances requises par les applications embarquées modernes. On recherche un convertisseur de haute précision permettant de reproduire avec fidélité les données des capteurs tout en maintenant une bande passante intéressante et une faible consommation de puissance.

Les objectifs secondaires permettant de remplir cet objectif principal sont :

1. Effectuer une revue de littérature sur l'état de l'art des ADC à suréchantillonnage. S'inspirer des résultats de la revue de littérature pour générer de nouvelles idées ;
2. Concevoir une nouvelle architecture d'ADC $\Delta\Sigma$ fonctionnelle à un haut niveau d'abstraction. On recherche une nouvelle structure de boucle présentant un bon potentiel pour atteindre de hautes performances et améliorer l'état de l'art actuel ;
3. Développer un ensemble de circuits électroniques permettant d'implémenter la nouvelle architecture d'ADC au niveau transistor avec la technologie CMOS 65 nm. Les circuits

conçus doivent être innovants et adaptés au besoin de l'ADC pour maximiser les performances et minimiser la consommation de puissance ;

4. Atteindre des spécifications supérieures ou comparables aux ADC de l'état de l'art.

CONTRIBUTIONS

Les principales contributions à la recherche de ce mémoire par articles sont les suivantes :

1. Une revue de littérature des récentes tendances en conception d'ADC à suréchantillonnage

Une revue de littérature élaborée des dernières avancées en matière d'ADC à suréchantillonnage a été effectuée. L'accent a été mis sur les techniques de conception utilisées dans les cinq dernières années dans toute la gamme des architectures d'ADC à suréchantillonnage : ΔΣ à temps discret, ΔΣ à temps continu, SAR à filtrage de bruit, zoom, incrémental, et ΔΣ dans le domaine temporel. Une comparaison en profondeur de ces topologies est présentée, mettant en lumière les techniques donnant les meilleures performances. De plus, les tendances au niveau de la conception des circuits, en particulier les amplificateurs et les structures de filtre de boucle sont explorés. De nouvelles conclusions sont tirées démontrant les limitations des conceptions actuelles et les tendances anticipées pour le futur. Ces nouvelles conclusions permettront de guider les chercheurs et les concepteurs du domaine pour pousser la recherche sur les ADC à suréchantillonnage vers de nouveaux horizons. Cette contribution a été publiée dans une revue scientifique :

[8] A. Verreault, P.-V. Cicek, et A. Robichaud, "Oversampling ADC: A review of recent design trends," *IEEE Access*, vol. 12, pp. 121 753–121 779, 2024.

2. Un ADC ΔΣ SMASH à annulation de bruit avec un étage SAR à filtrage de bruit

Cette contribution introduit une nouvelle architecture d'ADC ΔΣ SMASH qui annule le bruit de quantification grâce à la propriété de feedforward inhérente au SAR à filtrage de bruit (NS-SAR) utilisé comme deuxième étage. De plus, les erreurs de mismatch engendrées par l'étage NS-SAR sont filtrées par le premier étage, contournant le besoin d'une calibration additionnelle. L'élimination des circuits de calibration et d'annulation de bruit de même qu'une implémentation efficace du NS-SAR rendent cette nouvelle topologie très peu encombrante. Des simulations haut niveau démontrent le bon fonctionnement de la topologie avec un SQNR de 107.7 dB à un OSR de 14. La contribution a été présentée dans une conférence scientifique internationale :

[9] A. Verreault, P.-V. Cicek, et A. Robichaud, "A lean noise-cancelling sturdy MASH delta-sigma ADC with a noise-shaping SAR stage," dans *2023 30th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2023, pp. 1–4.

3. Un amplificateur CMOS rail-à-rail dynamique basse puissance pour les filtres à condensateurs commutés dans les ADC hautes performances

Un nouvel amplificateur dynamique optimisé pour les filtres à temps discret dans les ADC a été développé. L'architecture proposée inclut une compensation RC parallèle commutée qui est activée stratégiquement durant la phase d'échantillonnage pour minimiser la consommation de courant de l'amplificateur. La polarisation dynamique de l'amplificateur diminue d'autant plus la consommation d'énergie en diminuant les courants de slew rate durant la phase de convergence linéaire. Les simulations en CMOS 65 nm démontrent une réduction par 3.2 de la consommation de puissance par rapport à un amplificateur statique équivalent. Cette contribution a aussi été présentée dans une conférence scientifique internationale :

[10] A. Verreault, P.-V. Cicek, et A. Robichaud, "A rail-to-rail low-power dynamic CMOS amplifier for switched-capacitor filters in high-performance ADC," dans *2024 IEEE*

***67th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2024, pp. 1230–1234.**

4. Un ADC ΔΣ SMASH à annulation de bruit en CMOS 65 nm atteignant 500 kHz de bande passante et 90 dB de SNDR

Une implémentation en CMOS 65 nm de la nouvelle architecture d'ADC ΔΣ à annulation de bruit est proposée. L'étage du NS-SAR bénéficie d'un relâchement significatif des contraintes de conception par le filtrage de bruit additionnel apporté par le premier étage, permettant de maximiser l'efficacité en puissance. Une amélioration de l'amplificateur dynamique innovant est proposée pour optimiser le compromis taille/consommation de puissance dans le premier intégrateur du circuit. La réutilisation judicieuse des condensateurs du SAR du premier étage avec un ajustement de la tension de référence permet aussi d'implémenter un sommateur passif réduisant d'autant plus la consommation de puissance sans dégrader les performances. Les résultats de simulation démontrent d'excellentes spécifications avec une bande passante de 500 kHz et un SNDR de 90.3 dB à une consommation de puissance de 1.633 mW. Cette contribution a été acceptée pour présentation orale à la conférence internationale NEWCAS de L'IEEE qui aura lieu sous peu :

[11] A. Verreault, P.-V. Cicek, et A. Robichaud, "A 500 kHz-BW, 90 dB-SNDR lean noise-canceling SMASH delta-sigma ADC in 65 nm CMOS," dans *2025 23rd IEEE Interregional NEWCAS Conference (NEWCAS)*, in press.

CHAPITRE I

OVERSAMPLING ADC : A REVIEW OF RECENT DESIGN TRENDS

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1.1 RÉSUMÉ EN FRANÇAIS

Les convertisseurs analogiques-numériques à suréchantillonnage constituent la base des interfaces de données haute performance et haute précision en raison de leur remarquable capacité à filtrer le bruit de quantification. Cette caractéristique en fait le choix privilégié pour les applications nécessitant un rapport signal sur bruit (SNR) élevé et une bande passante modérée, tout en offrant une grande flexibilité de conception. Cet article propose une revue approfondie des avancées récentes en matière d'ADC à suréchantillonnage dédié à ces applications. Spécifiquement, la revue de littérature se concentre sur les techniques de conception utilisées au courant des 5 dernières années en couvrant toute la gamme des architectures d'ADC à suréchantillonnage : $\Delta\Sigma$ à temps discret, $\Delta\Sigma$ à temps continu, SAR à filtrage de bruit, zoom, incrémental, et $\Delta\Sigma$ dans le domaine temporel. Une comparaison détaillée de ces différentes topologies est présentée, mettant en lumière les designs qui atteignent les meilleures figures de mérite. De plus, ce papier explore les tendances de conception au niveau circuit qui sont utilisées dans ces architectures, avec une attention particulière aux amplificateurs et aux structures de filtre de boucle. De nouvelles conclusions sont tirées démontrant les limitations de la plupart des travaux de recherche dans le contexte de l'implémentation d'ADC dans des

systèmes complets, tout en donnant un aperçu des tendances anticipées qui façonneront le domaine dans le futur.

1.2 ABSTRACT

Oversampling ADC serve as the backbone of high-performance, high-precision data interfaces, owing to their remarkable ability to filter out quantization noise. This attribute makes them the preferred choice for applications requiring high signal-to-noise ratio (SNR) and moderate bandwidth, with great design flexibility. This paper provides an extensive survey of the latest advancements in oversampling ADC tailored for such applications as documented in recent literature. Specifically focusing on design techniques employed within the last five years, the survey encompasses various oversampling ADC architectures, including discrete-time and continuous-time $\Delta\Sigma$, noise-shaping SAR, zoom, incremental, and time-domain modulators. A thorough performance comparison between these different topologies is presented, highlighting designs that achieve the best figures-of-merit. Furthermore, the paper explores circuit-level design trends commonly shared among these architectures, with particular attention given to amplifier designs for loop filters. Conclusions drawn highlight the limitations of much of the research works in the context of implementing ADC within complete systems, while also providing insight into the expected future trends that will shape the field moving forward.

1.3 INTRODUCTION

The relentless advance of semiconductor technology has brought in an era of increasingly efficient digital signal processing as CMOS technology nodes continue to shrink. This progression has led to remarkable improvements in computational power, speed, and energy efficiency, making signal processing in the digital domain the preferred approach in modern

electronic systems. Nevertheless, the physical world operates in the analog domain, necessitating cutting-edge analog interfaces to fully leverage the benefits of digital signal processing. Consequently, analog-to-digital converters (ADC) can quickly become bottlenecks in the signal chain if they are not specified and designed with great care.

To meet the demands of modern electronic systems, research on improving ADC circuits in terms of resolution, power efficiency, noise reduction, speed, accuracy, and miniaturization is relentless. Among all the proposed solutions and topologies, the delta-sigma ($\Delta\Sigma$) configuration is of particular interest. By cleverly combining feedback error correction and oversampling to push quantization noise outside of the signal band, the $\Delta\Sigma$ architecture allows for very high precision using electronic blocks with looser specifications than with alternate ADC topologies.

Although the original concepts of $\Delta\Sigma$ modulation date back to the early 1960s [12, 13, 14], $\Delta\Sigma$ converters (and oversampling ADC in general) remain a primary research focus for high signal-to-noise-and-distortion ratio (SNDR) applications. The prevalence of oversampling converters among designs with a SNDR above 80 dB, as illustrated in Fig. 1.1, underscores their critical role in achieving high precision and high performance in ADC design, especially in recent years. The ADC data points are sourced from Murmann's database[15] which comprises data from the International Solid-State Circuits Conference (ISSCC) and the IEEE VLSI Technology Symposium from 1997 to 2023. The black diamond datapoints on the figure represent the ADC designs studied in this review paper, all of them oversampling topologies gathered from various IEEE journals and conferences published in the past 5 years.

With such a clear trend, it should be no surprise that oversampling ADC stand out as the go-to in high-precision, low-bandwidth applications. For instance, high-performance $\Delta\Sigma$ ADC are often used in wireless sensor nodes, precision industrial and research process

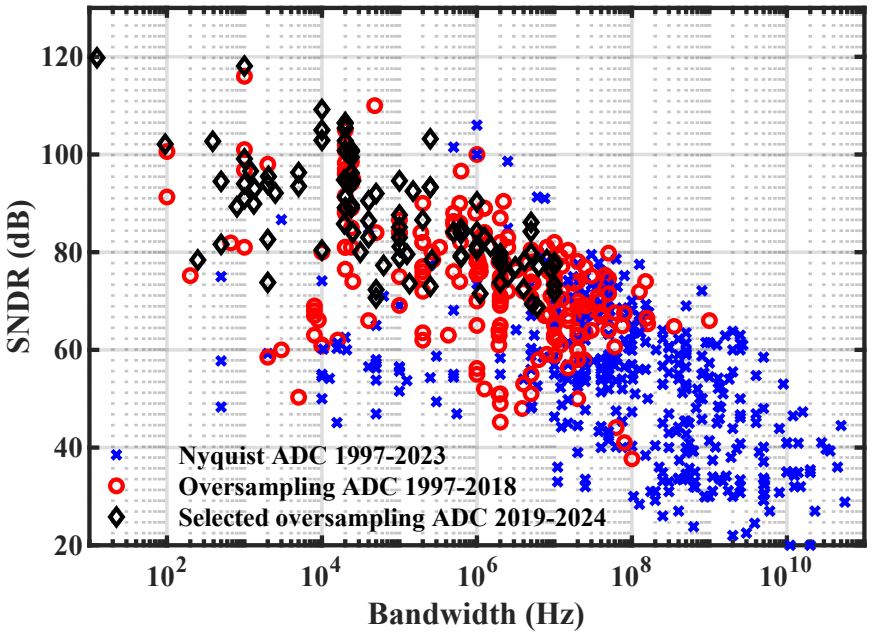

FIGURE 1.1 : Scatter plot illustrating the relationship between SNDR and bandwidth for the selected oversampling ADC and those from Murmann's database.

instrumentation or high-fidelity audio processing. However, such applications demand not only high SNDR, but also low power consumption (given that many of these systems are battery-powered) and cost effectiveness (to facilitate widespread adoption). Satisfying these requirements imposes strict design constraints, which have been the focus of numerous research endeavors. Hence, this review paper aims to explore recent trends in oversampling ADC where research emphasis lies not on maximizing bandwidth, but rather on enhancing SNDR at minimal cost and power overhead.

The paper is structured as follows. Firstly, section 1.4 presents the methodology. Section 1.5 then provides a concise review of $\Delta\Sigma$ modulation and an introduction to the different oversampling ADC topologies. Next, section 1.6 offers an overview of the current state of the art, including a comparison of key figures-of-merit (FOM) and performance metrics. Subsequently, sections 1.7 and 1.8 explore in depth system-level and circuit-level design trends, respectively. Section 1.9 discusses system-on-chip (SoC) implementation and ADC

benchmarking, shedding light on FOM limitations. Finally, section 1.10 summarizes the main findings and presents future perspectives.

1.4 METHODOLOGY

To ascertain the prevailing trends in oversampling ADC design tailored for high-precision applications, an exhaustive review was conducted throughout prominent IEEE journals and conferences spanning the past five years. Only oversampling ADC designs deemed suitable for high-precision and moderate bandwidth applications were considered, discarding those with an effective number of bits (ENOB) below 11 bits and those with a bandwidth in excess of 10 MHz. Numerous applications require ADC performance within these specifications[7, 16, 17, 18, 19]. For instance, sensor data acquisition in Internet of things (IoT), sensor nodes and industrial process instrumentation demands high precision, often well over 11 bits. Depending on the nature of the signals involved, bandwidth can vary from a few hertz for temperature or humidity detection to megahertz for ultrasound imaging. Signal processing in audio and biomedical monitoring applications is also notable for requiring high accuracy, but moderate bandwidth. Furthermore, low-bandwidth, low-power communication protocols benefit from such specifications with highly efficient oversampling ADC.

The lower cutoff ENOB limit of 11 bits is selected since simpler Nyquist ADC are able to achieve ENOB up to 10 to 12 bits with standard manufacturing process matching. Beyond this precision level, calibration or other special design techniques are required to improve accuracy, enhancing the attractiveness of the oversampling ADC alternative. This survey focuses on energy efficiency enhancement and implementation cost reduction, rather than bandwidth boosting, which is not a critical factor for the target applications considered.

The scrutinized publications include the Journal of Solid-State Circuits (JSSC), IEEE Transactions on Circuits and Systems I & II (TCAS I & II), IEEE Transactions on VLSI Systems, Solid-State Circuit Letters, as well as the International Solid-State Circuits Conference (ISSCC) and Custom Integrated Circuits Conference (CICC). Additionally, five papers sourced from Murmann's database [15] were considered, despite dating from more than five years, since their performance still rivals even the latest state-of-the-art designs. Each selected paper presents a physical tape-out implementation and corresponding measurement results.

The analysis and discussion in this survey revolve around the design techniques used in the selected works, which are grouped by topology, with the main innovations and design trends identified. All techniques discussed have been used in some of the selected state-of-the-art designs.

1.5 OVERVIEW OF OVERSAMPLING ADC STRATEGIES

This section will cover the basics of oversampling ADC. The principle of operation of this ADC category will be demonstrated using the quintessential oversampling topology, the discrete-time (DT) $\Delta\Sigma$ ADC. Following this, we will introduce and discuss the various other oversampling ADC topologies featured in this review.

The principle of operation of oversampling ADC is to convert numerous successive low bit-count samples into a single high-resolution output, thus earning its designation as an *oversampling* ADC. By incorporating the quantizer component within an error-correcting feedback loop, precision can be significantly enhanced.

For readers new to this field, some excellent textbooks offer more in-depth insight into the inner workings of this ADC family [7, 20].

1.5.1 THE DISCRETE-TIME ΔΣ MODULATOR

Fig. 1.2 depicts the block schematic of the DT version of the ΔΣ ADC. The conversion process begins with the sample-and-hold (S/H) stage, which discretizes the analog input signal in time. Subsequently, the signal undergoes low-pass filtering through the loop filter F(z). This circuit block serves as the error correction element in the feedback loop and is commonly implemented using a switched-capacitor integrator circuit. Following this, the signal enters a quantizer, typically a flash ADC[21] with a low bit-count (1 to 4 bits). The feedback path features a digital-to-analog converter (DAC) allowing for the subtraction of the digital output of the quantizer Y(z) from the analog input $V_{in}(z)$. This DAC is one of the most critical blocs in the architecture as any error or distortion it introduces are not shaped by the error-correcting loop due to its placement in the feedback path. The high-frequency digitized data stream Y(z) is finally converted into a lower frequency, high bit-count output data $D_{out}(z)$ by means of a decimation filter. The ratio of decimation, equal to the sampling frequency ratio between Y(z) and $D_{out}(z)$, is known as the oversampling ratio (OSR). All things being equal, increasing OSR enhances ADC precision. However, this represents a key trade-off in ΔΣ ADC design, as higher OSR improves SNDR but reduces bandwidth for the same power consumption.

The low bit-count quantizer, due to its coarse voltage steps, introduces substantial errors termed quantization noise and denoted e(z) in Fig. 1.2. Classic feedback theory can be applied

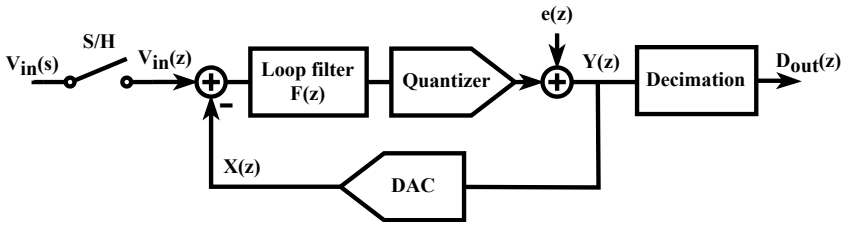

FIGURE 1.2 : Block diagram of the DT ΔΣ ADC.

to derive ADC transfer functions for both input $V_{in}(z)$ and quantization noise e(z), designated respectively as signal transfer function

$$STF(z) = \frac{Y(z)}{V_{in}(z)} = \frac{F(z)}{1+F(z)} = z^{-1} \tag{1.1}$$

and noise transfer function

$$NTF(z) = \frac{Y(z)}{e(z)} = \frac{1}{1+F(z)} = 1-z^{-1}, \tag{1.2}$$

where

$$F(z) = \frac{z^{-1}}{1-z^{-1}} \tag{1.3}$$

is the transfer function of an ideal integrator loop filter.

With these equations plotted in Fig. 1.3, it becomes clear that the error signal undergoes strong filtration, while the input signal is unaffected. As highlighted with the blue shading, the remaining noise in the signal band is significantly attenuated by high-pass filtering through the feedback loop, an effect commonly referred to as noise shaping. Indeed, at the ADC output, the decimation filter acts as a sharp low-pass filter, effectively removing residual noise above the signal band. To achieve sharper noise shaping, a higher-order loop filter may be used, which can be performed simply by cascading additional switched-capacitor integrators. Higher-order noise shaping may reduce the OSR required to meet specific SNDR requirements, albeit at the cost of critical stability challenges.

Fig. 1.4 illustrates the transient waveforms of a 1st-order DT $\Delta\Sigma$ ADC. Both sampling frequency and amplitude are normalized to 1 Hz and ±1 V, respectively. Input $V_{in}(s)$ is a sinusoid with a frequency one-thousandth that of the sampling frequency. OSR is set to 32 and the quantizer has 9 levels. Modulator output Y(z), prior to decimation, presents a rapidly

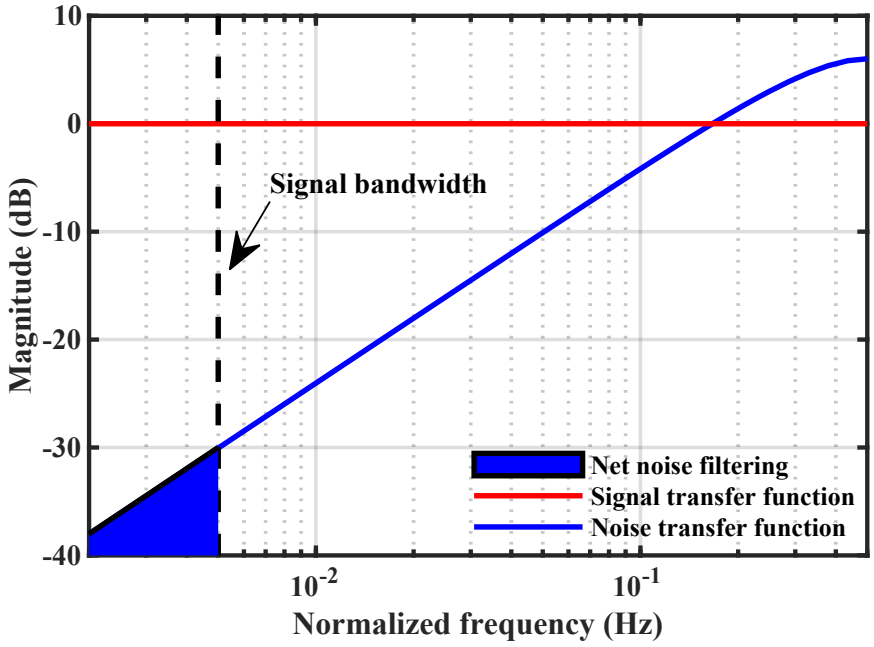

FIGURE 1.3 : Signal and noise transfer function of a typical ΔΣ ADC. The shaded region shows the total shaping of the quantization noise from both the loop filter and the decimation filter.

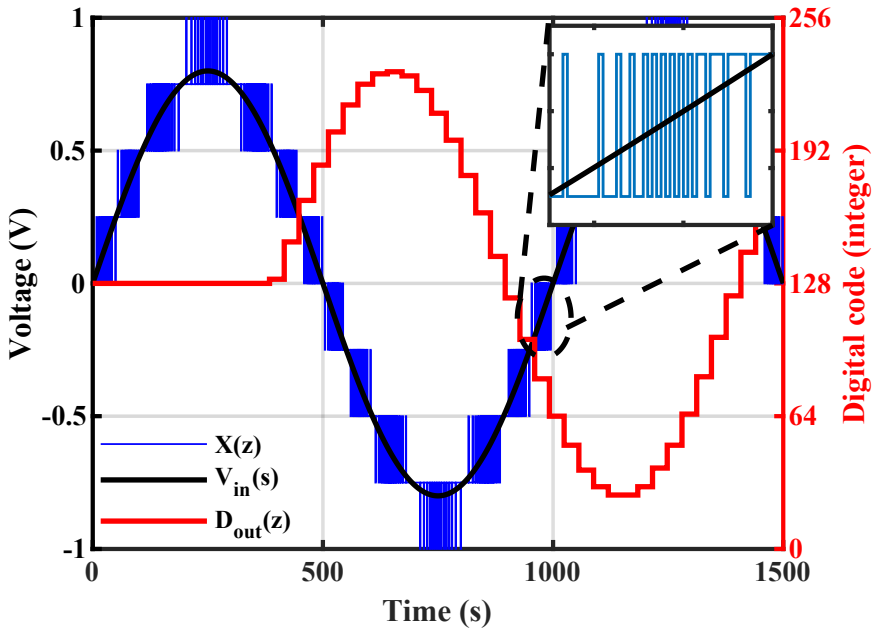

FIGURE 1.4 : Simulated transient waveforms of a 1st-order ΔΣ ADC with 9 quantizer levels for signals labelled in Fig. 1.2.

varying low-resolution digital stream, which, for visual convenience, is illustrated through DAC output X(z) on the figure. The error-correcting loop ensures that the mean value of X(z) closely tracks input $V_{in}(s)$. Notably, upon zooming into the rising slope of the input sinusoid, it becomes evident that bits are predominantly low at the onset and tend to shift high more often later since the amplitude of the input has risen. After decimation, output $D_{out}(z)$ yields a slower, high-resolution digital code.

One notable limitation of ΔΣ ADC, clearly depicted in the figure, is the substantial delay imposed by the decimation filter before the high-resolution sample is accessible at the output. A solution for this latency issue, which will be covered in detail in a subsequent section, is to use an incremental ΔΣ architecture. In such a structure, the memory elements of the integrators and of the decimation filter are reset after each conversion, eliminating the conversion latency.

1.5.2 THE CONTINUOUS-TIME ΔΣ MODULATOR

Fig. 1.5 illustrates the continuous time (CT) variant of the ΔΣ ADC. Unlike its DT counterpart, the input remains in the analog domain and is not sampled before entering the loop. Nevertheless, sampling still needs to take place within the quantizer, which requires clocking. In this configuration, the loop filter typically takes the form of an active RC filter. A significant advantage of this setup is its intrinsic anti-aliasing property, a consequence of

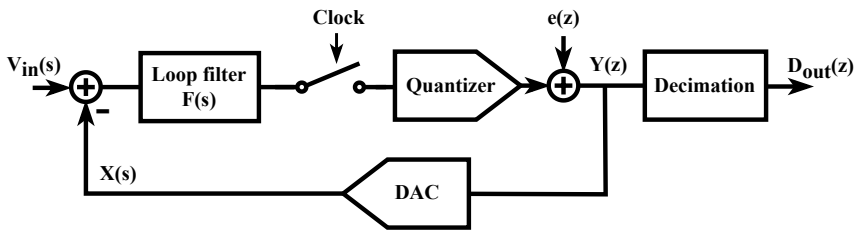

FIGURE 1.5 : Block diagram of the CT ΔΣ ADC.

the filtering operation preceding the sampling. Detailed discussions about this phenomenon and the derivation of loop filter equations can be found in [7]. The CT ΔΣ modulator is easier to drive because its input impedance is resistive, unlike the switched-capacitor input stage of the DT ΔΣ. As for noise shaping, it occurs analogously to the DT case. However, the CT architecture is not devoid of drawbacks, including sensitivity to process variations. Indeed, in the CT architecture, the integration constants depend on the RC time constant, which is more liable to be affected by fabrication variations compared to the easily matchable capacitor ratios used in the DT architecture. Additionally, the CT nature of the circuit heightens sensitivity to jitter and DAC waveform symmetry.

1.5.3 THE INCREMENTAL ΔΣ MODULATOR

The incremental ΔΣ ADC, initially proposed with a current-mode input in [22] and further refined in [23], is a variant of the conventional ΔΣ architecture. In this topology, the memory elements of the loop filter and the decimation filter are reset for each conversion as depicted in Fig. 1.6, resulting in a Nyquist rate ADC. This resetting of memory elements eliminates output delays, facilitates multiplexing of inputs from an array of sensors and enables implementation of sleep mode between acquisition periods. The formation of idle tones with DC input is also alleviated [7]. Moreover, the decimation filter in the incremental variant is implemented as a simple finite impulse response (FIR) filter instead of the usual infinite impulse response (IIR) filter. Optimal filtration is achieved by weighting the filter more heavily with the first samples and less with the last ones. Indeed, this weighting is optimal because the quantization noise from the last few samples is not shaped by subsequent samples which will serve for the next conversion[7]. However, it is worth noting that the reduced weighting in the incremental variant leads to inferior thermal noise performance compared to conventional ΔΣ ADC. While conventional ΔΣ ADC benefit from a thermal noise reduction by a factor of OSR,

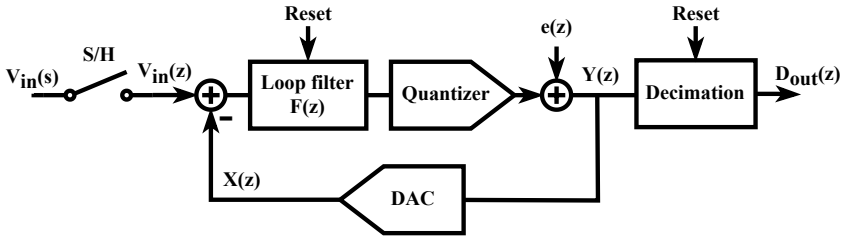

FIGURE 1.6 : Block diagram of the incremental ΔΣ ADC.

the incremental variant experiences a less pronounced reduction, especially with higher-order modulators [18]. Consequently, to meet a given SNR specification, the incremental modulator consumes more power, as higher capacitive loads are required to mitigate thermal noise. Detailed noise analysis and design considerations for incremental ΔΣ ADC are provided in [24, 25, 26].

1.5.4 THE NOISE-SHAPING SAR TOPOLOGY

The successive approximation (SAR) ADC[21] is a Nyquist ADC which performs a binary search algorithm to discretize signals. It reutilizes the same comparator for every successive comparison, with one comparison per output bit. The SAR ADC is highly efficient, especially in its typical implementation with a capacitive DAC (CDAC). However, at higher precision, the capacitive loading and the area occupied by the CDAC increase significantly, as the capacitor size doubles with each additional bit. Additionally, maintaining low comparator noise becomes more challenging, often requiring a power-hungry preamplifier before the comparator to achieve the necessary accuracy.

An approach to improve the SAR ADC precision without excessive comparator and capacitor requirements is to use it in an oversampling topology : the noise-shaping SAR (NS-SAR). This topology is a relatively recent oversampling ADC architecture introduced

in 2012 [27]. It differs from traditional ΔΣ ADC in several key ways. Its unique features include : 1) the direct sampling and quantization of the input signal by the SAR quantizer, which typically uses a higher bit-count than conventional ΔΣ designs ; 2) the precise extraction of the residue error at the end of the SAR conversion, which is determined from the remaining voltage on the SAR CDAC array ; and 3) the feedback mechanism that conveys only the residue error instead of the full modulator output[28]. High bit-count quantization, as well as only needing to process the residue error, allow the linear blocks of the filter to handle signals with very low swing, significantly easing design constraints.

Fig. 1.7 illustrates the two main NS-SAR topologies : error feedback (EF)[29] and cascaded integrator feed-forward (CIFF)[27]. The fundamental distinction between these architectures lies in the feedback return path : the EF structure feeds back into the CDAC array, while the CIFF structure feeds back into the comparator as an additional offset. This difference affects noise shaping to yield two alternate transfer functions :

$$NTF_{EF}(z) = 1 - H_{EF}(z)z^{-1}, \tag{1.4}$$

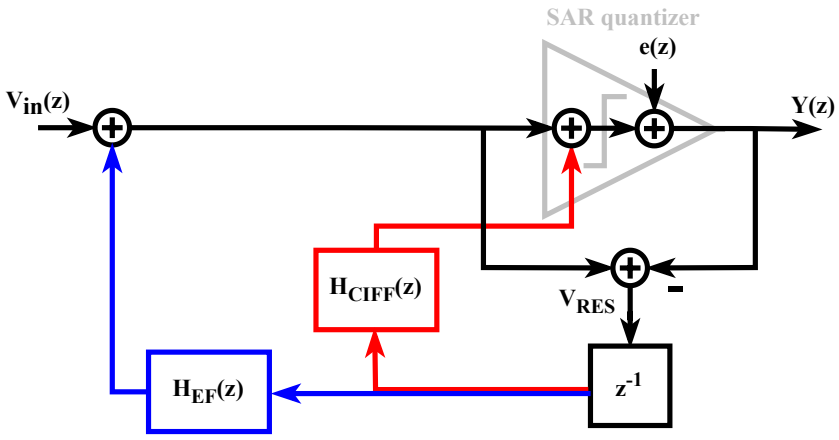

FIGURE 1.7 : Block diagram of the NS-SAR ADC.

$$NTF_{CIFF}(z) = \frac{1}{1 + H_{CIFF}(z)z^{-1}}. \tag{1.5}$$

In (1.4), the EF case, $H_{EF}(z)$ appears in the numerator, facilitating its implementation through a straightforward FIR filter to achieve the desired noise shaping. However, $NTF_{EF}(z)$ is sensitive to gain variation, as filter coefficients may drift and degrade performance. Conversely, in (1.5), the CIFF case, $H_{CIFF}(z)$ resides in the denominator, necessitating the use of an integrator or IIR filter to achieve a proper high-pass filter $NTF_{CIFF}(z)$, increasing circuit complexity. However, while a sufficiently high gain is required, it need not be precisely tuned, thus relaxing matching constraints compared to the EF case [28]. Combined implementations of both EF and CIFF filter structures have been proposed [30], resulting in a total NTF derived from the multiplication of (1.4) and (1.5).

1.5.5 THE ZOOM TOPOLOGY

The zoom topology, pioneered by Souri and Makinwa in the early 2010s [31, 32], stands out as the ideal architecture for achieving high precision in low-bandwidth applications. Illustrated in Fig. 1.8, this architecture closely resembles the two-step ADC[21]. Initially, a Nyquist ADC performs coarse quantization, typically using a SAR ADC of 4 to 6 bits.

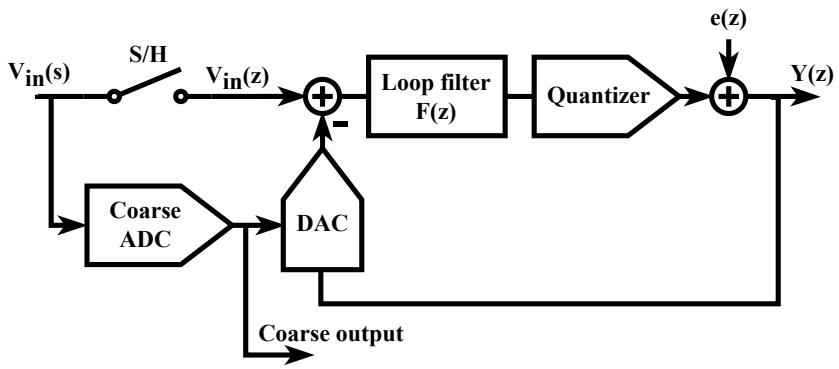

FIGURE 1.8 : Block diagram of the zoom ADC.

Subsequently, a fine quantization stage employs an incremental ΔΣ in which the feedback DAC output range is dynamically adjusted based on the coarse quantization results. This significantly reduces the resolution requirement of the ΔΣ stage as the feedback DAC range narrows within a few coarse LSB of the input signal. Hence, selecting a single-bit quantizer is a common design choice due to its inherent linearity. Furthermore, the loop filter is subjected to a minimal input swing thanks to the output of the feedback DAC being zoomed in close proximity to the input level, facilitating simple and power-efficient loop filter amplifier design. A key distinction from conventional two-step ADC is the absence of explicit residue signal computation, which typically introduces offset, gain, and linearity errors through amplification and subtraction circuitry before the fine quantization stage [32].

1.5.6 THE TIME-DOMAIN ΔΣ MODULATOR

In the context of this survey, a *time-domain* (TD) ΔΣ modulator refers to a ΔΣ ADC where all or part of the signal processing occurs in the time domain instead of the conventional voltage amplitude domain. The time-encoded information can be represented as frequency, phase, or pulse-width modulation (PWM). The primary objective of this configuration is to achieve a digital-like design that leverages advancements in technology scaling for improved speed and power efficiency. This approach can prove particularly advantageous in deep submicron technology nodes where maintaining accuracy in voltage domain quantizers and filters becomes more challenging at low supply voltage, whereas time-domain accuracy improves due to reduced transition times. However, the typical voltage-controlled oscillators (VCO) used for processing data in the time domain are nonlinear, often requiring the use of calibration and/or linearization techniques[33].

Fig. 1.9 illustrates a typical configuration of TD ΔΣ ADC. The loop filter can be implemented either using a classical CT integrator or a VCO-based TD integrator. The

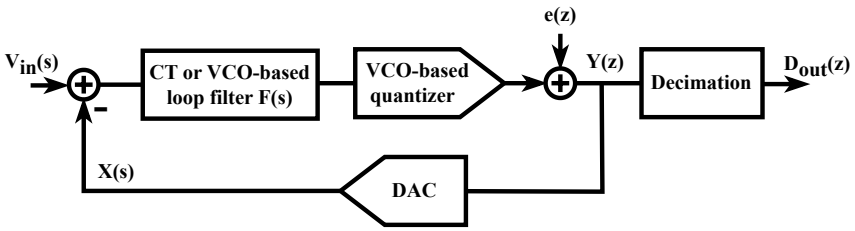

FIGURE 1.9 : Block diagram of a typical TD ΔΣ ADC.

quantizer is VCO-based and often also contains a digital backend, which includes a counter and additional processing. Accumulating the VCO output in a counter provides intrinsic signal integration, resulting in inherent first-order noise shaping to complement the noise shaping of the loop filter. An overview of different TD ΔΣ ADC architectures is presented in [34] while detailed exploration of the recent state-of-the-art design trends is covered in later sections of this paper.

1.6 STATUS OF THE STATE OF THE ART

1.6.1 COMPARISON WITH OLDER DESIGNS AND NYQUIST ADC

The oversampling ADC targeted in this review paper are compared with various Nyquist and older oversampling ADC designs from Murmann's database [15] in Fig. 1.10. The scatter plot relates energy per conversion to ENOB, visually illustrating the trade-offs between ADC resolution and conversion efficiency.

Trade-offs can also be quantified using FOM, taking into account key performance metrics such as SNDR, bandwidth, and power consumption. Among the most commonly used FOM for oversampling ADC are Schreier's [7] :

$$FOM_{Sc} = SNDR + 10\log\frac{BW}{P}, \tag{1.6}$$

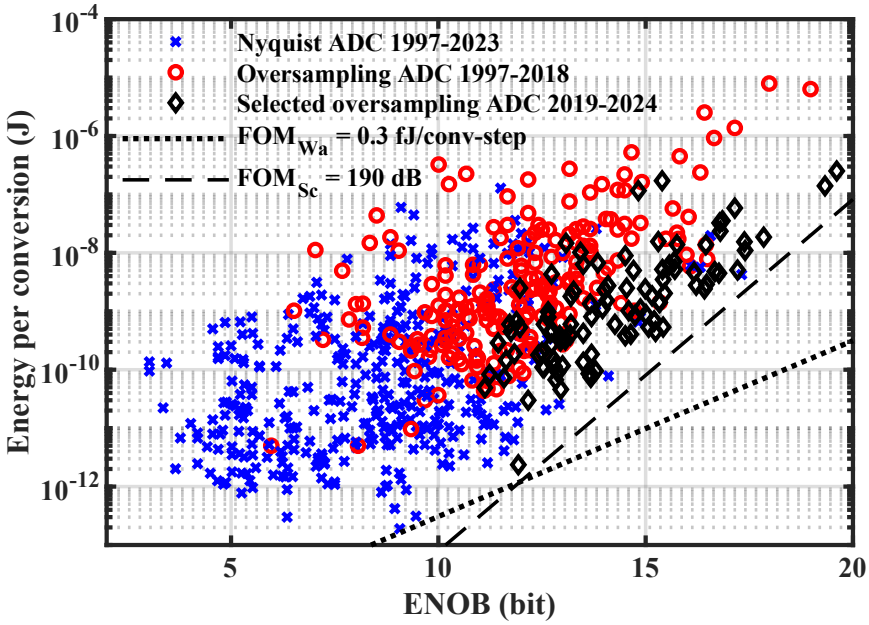

FIGURE 1.10 : Scatter plot illustrating the trade-off between conversion efficiency and resolution for the selected oversampling ADC and those from Murmann's database.

and Walden's [35, 36] :

$$FOM_{Wa} = \frac{P}{2^{ENOB} F_s}, \tag{1.7}$$

where

$$ENOB = \frac{SNDR - 1.76}{6.02}, \tag{1.8}$$

BW is the ADC bandwidth, P is the power consumption and F_s is the Nyquist sampling frequency. Isolating the energy as P/F_s in (1.6) and (1.7) allows for the plotting of the corresponding slopes in Fig. 1.10. Consequently, we observe that the most optimal designs, exhibiting the highest FOM, tend to cluster towards the lower right corner of the scatter plot along the slopes of the FOM. Indeed, the state-of-the-art frontier closely follows the slope of FOM_{Sc} at high ENOB and FOM_{Wa} at lower ENOB, suggesting that these FOM effectively encapsulate relevant design trade-offs. Furthermore, the figure highlights that oversampling

ADC feature superior precision due to their inherent noise-shaping capabilities. The selected designs clearly rank among the top performers.

1.6.2 SELECTED OVERSAMPLING ADC

Fig. 1.11 dives deeper into the selected ADC from the previous figure, specifying their topologies : DT ΔΣ, CT ΔΣ, NS-SAR, TD ΔΣ and hybrid designs incorporating both voltage-domain and time-domain stages. The five data points depicted in red, as opposed to the usual color, represent older designs sourced from Murmann's database that are still competitive with the state of the art of the last 5 years and are thus selected for analysis in this paper. Also, gray triangles represent state-of-the-art designs identified in a previous survey from 2015 [16].

Remarkably, there has been a significant enhancement in energy efficiency over the past decade. Many recent designs consume less than a tenth of the energy per conversion while maintaining similar precision compared to state-of-the-art designs from 2015. The designs boasting the highest FOM are identified in the figure, featuring either or both of FOM_{Wa} below 6.5 fJ/conv-step [37, 38, 39, 40, 41] and FOM_{Sc} in excess of 183 dB [41, 42, 43, 44, 45, 46, 47, 48, 49, 50].

From a system-level perspective, NS-SAR designs are the top performers at low ENOB. This is demonstrated by the cluster of stars along the FOM_{Wa} slope between ENOB of 12 and 14 bits in the figure. Between ENOB of 14 and 17 bits, various topologies compete for supremacy. Interestingly, the designs by Lee [46] and Liu [47] stand out as the only DT ΔΣ converters offering truly cutting-edge performance. For designs requiring precision beyond ENOB of 17 bits, the zoom architecture emerges as the clear leader.

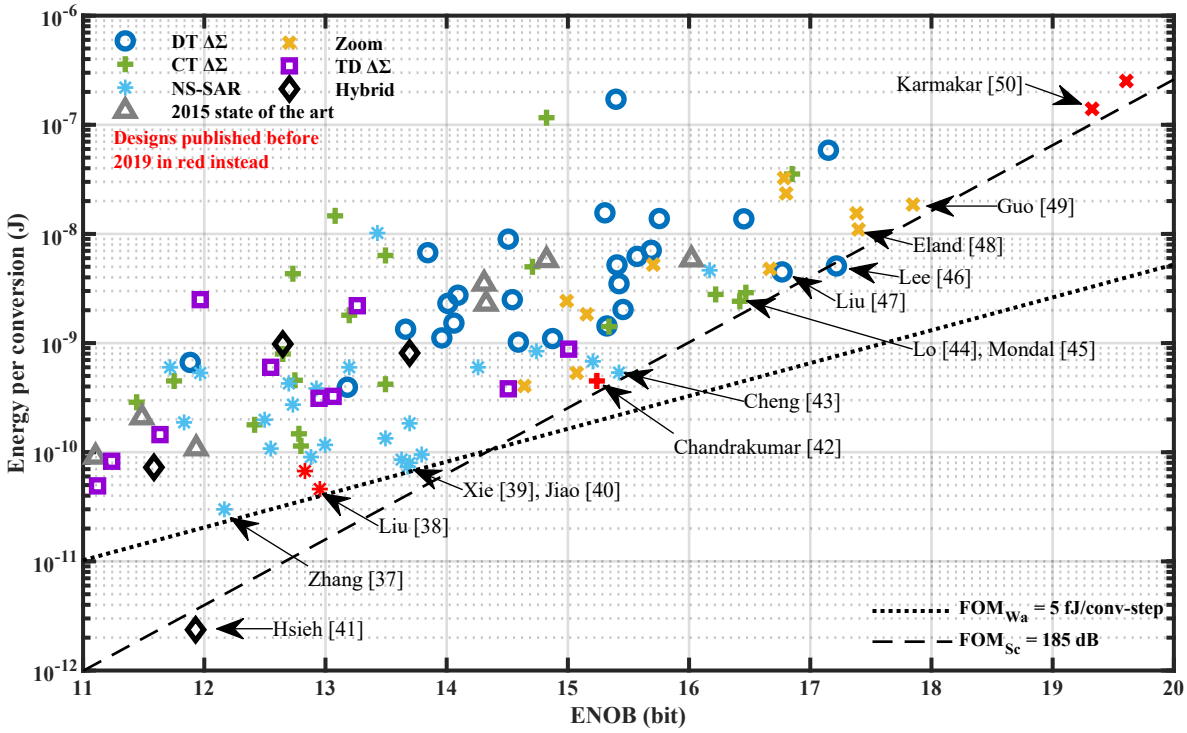

FIGURE 1.11 : Scatter plot showcasing the energy/resolution trade-off for the selected ADC with their respective architectures highlighted. Designs with the highest figures of merit are labelled on the plot.

TD ΔΣ converters exhibit comparatively mediocre power efficiency, as no design comes close to the FOM boundaries shown in the figure. Additionally, the nonlinearity issues of the VCO commonly used in this topology prevent these converters from achieving an ENOB higher than 15 bits. In contrast, every other topology features designs with resolutions exceeding this threshold. Nevertheless, the TD topology remains of interest because it holds significant potential for improvement with recent and upcoming technology nodes, given its compatibility with digital-friendly circuits. Furthermore, hybrid designs including a TD stage are already demonstrating impressive results with Hsieh's highly efficient design[41].

An important piece of information missing from Fig. 1.11 and the prior discussion is bandwidth performance. Focusing solely on the precision vs. energy per conversion tradeoff

disregards the value of faster designs, as techniques for higher-speed circuits are generally expected to be more complex, thus to consume more power and require a larger area footprint. Hence, Fig. 1.12 presents architecture performance relative to conversion speed, by displaying FOM_{Sc} of all the designs in Fig. 1.11, but according to bandwidth as the x-axis.

Similarly, Fig. 1.13 presents the bandwidth and ENOB specifications of the top sixty designs that surpass a FOM_{Sc} of 172 dB. The highlighted areas indicate the design space occupied by each topology, illustrating the trade-offs between bandwidth and precision for each family.

Some clear trends emerge by inspecting these three figures. For higher bandwidth, ranging from 100 kHz up to the 10 MHz limit of this survey, NS-SAR designs dominate performance, particularly at moderate ENOB. As anticipated, the fastest designs exhibit a

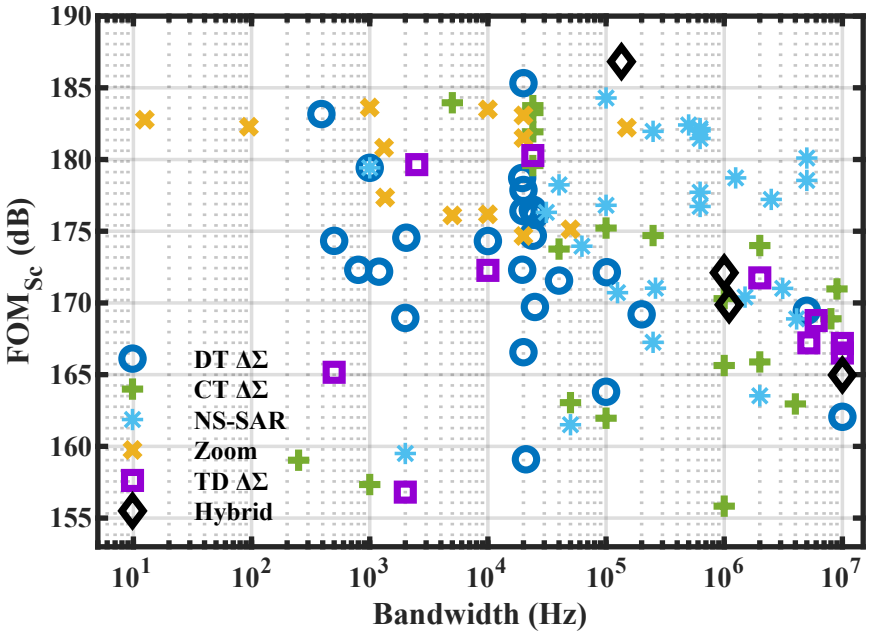

FIGURE 1.12 : Scatter plot illustrating the FOM_{Sc} of the selected ADC in terms of bandwidth with their respective architectures highlighted.

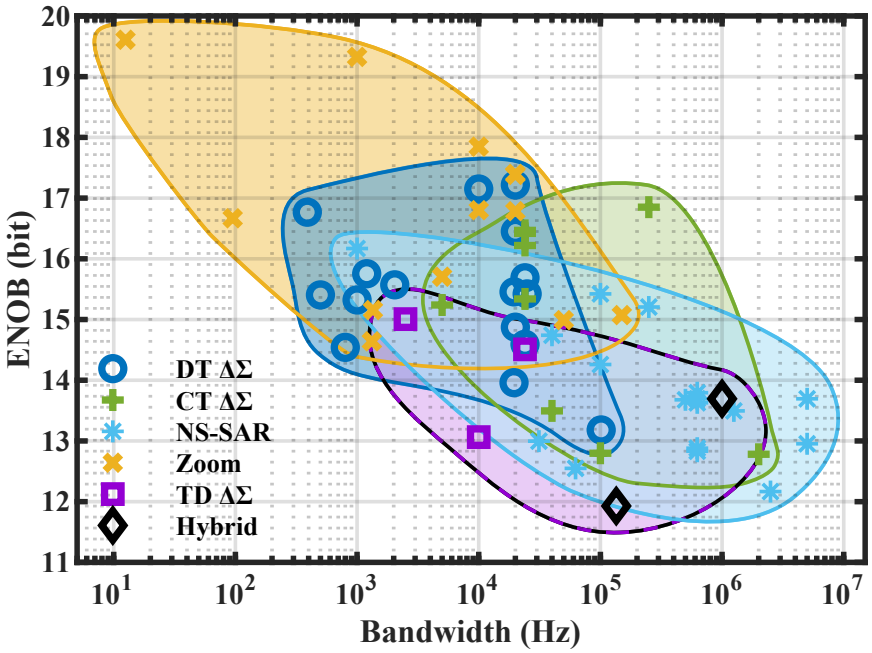

FIGURE 1.13 : Scatter plot indicating ENOB and bandwidth for the top sixty selected ADC (FOM_{Sc} > 172 dB). The zone of optimal operation for each architecture family is highlighted.

slight reduction in peak FOM_{Sc}, with only Liu's design[38] managing to surpass 180 dB above 1 MHz. In the intermediate bandwidth range of 5 kHz to 100 kHz, top performance is shared between CT and DT ΔΣ, as well as zoom architectures. While zoom architectures excel in achieving high ENOB, DT and CT ΔΣ designs lead the moderate to high ENOB space, with CT designs generally demonstrating higher bandwidth. Finally, for bandwidths below 5 kHz, zoom architectures clearly dominate, aside from the DT ΔΣ design by Liu[47], which presents state-of-the-art performance in this range.

Once more, most TD ΔΣ and their hybridization with other topologies lag slightly behind in terms of performance. However, their ability to reach high bandwidth due to their TD digital-like processing circuit is clearly illustrated by the group of purple squares and black diamonds on the far right of Fig. 1.12. Maturation of these budding approaches can be expected to yield more competitive performance in the future.

The subsequent sections of the paper delve into the analysis of the design trends studied in the ADC implementations of Fig. 1.11 and Fig. 1.12, starting with a system-level perspective and thereafter honing in on circuit-level techniques.

1.7 SYSTEM-LEVEL DESIGN TRENDS

1.7.1 DESIGN TRENDS IN THE CONVENTIONAL DISCRETE-TIME AND CONTINUOUS-TIME ΔΣ TOPOLOGIES

THE MULTI-STAGE NOISE-SHAPING TECHNIQUE

The primary design considerations in a conventional ΔΣ architecture revolve around the power/precision trade-off for a given bandwidth constrained by OSR. To benefit from a more favorable trade-off, many designs opt to increase the modulator's noise-shaping order, allowing for a reduction in OSR while maintaining SNDR. However, at higher order, stabilizing the feedback loop becomes increasingly challenging, as the modulator may exhibit instability at high input amplitudes, limiting the practical input range[7]. Addressing this challenge, a clever technique known as multi-stage noise shaping (MASH) was introduced in [51]. This approach involves cascading multiple noise-shaping loops to achieve high-order noise shaping without encountering stability issues. In this method, the quantization error from the first stage is fed into a second noise-shaping modulator stage. The digitized error is ultimately subtracted from the output of the first stage, as depicted in Fig. 1.14. Additional digital filters are required before the subtraction to ensure proper quantization noise filtration. The resulting transfer function is expressed as :

$$Y_{out}(z) = H_1 Y_1 - H_2 Y_2. \tag{1.9}$$

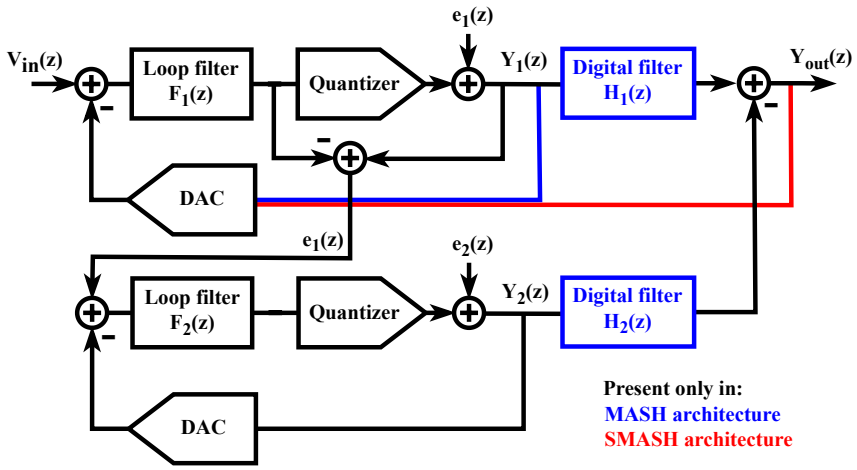

FIGURE 1.14 : Block diagram of the multi-stage noise-shaping (MASH) and the sturdy multi-stage noise-shaping (SMASH) ΔΣ ADC architectures.

Replacing Y_1 and Y_2 for the noise and signal transfer functions gives :

$$Y_{out}(z) = H_1 STF_1 V_{in}(z) + H_1 NTF_1 e_1(z) - H_2 STF_2 e_1(z) - H_2 NTF_2 e_2(z). \tag{1.10}$$

Designing digital filters H_1 and H_2 to meet the condition

$$H_1 NTF_1 = H_2 STF_2 \tag{1.11}$$

yields :

$$Y_{out}(z) = STF_1 STF_2 V_{in}(z) - NTF_1 NTF_2 e_2(z). \tag{1.12}$$

As a result, MASH effectively nullifies the error from the initial stage, e_1, leaving behind solely the error introduced by the second stage quantizer, e_2, which undergoes substantial attenuation by both NTF. Despite its inception in the 1980s, contemporary designs frequently adopt this strategy, amalgamating stages based on diverse architectures such as NS-SAR, TD, and conventional CT / DT ΔΣ modulators [40, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62]. Leveraging this approach incorporating a Nyquist converter as either the first stage (0-Xth order modulator) or the second stage (X-0th order modulator) can also be a great technique to improve performance. On one hand, the use of a 0-X MASH narrows the input range of the ΔΣ

modulator [54, 63], relaxing design constraints in a manner similar to a zoom ADC. On the other hand, the X-0 MASH enhances SNDR in a power-efficient manner by simplifying the second stage design[52]. For example, in [52], a 2-0 architecture is employed. Instead of solely relying on a SAR ADC for the second stage, it is also repurposed as a digital feedforward to diminish the modulator's input range, which relaxes the loop filter constraints and culminates in achieving a state-of-the-art FOM_{Sc} of 179.4 dB.

THE STURDY MULTI-STAGE NOISE-SHAPING TECHNIQUE

A significant drawback of MASH lies in the stringent requirement to precisely match the transfer function of the second-stage digital filter, H_2, to the analog NTF_1 of the first stage, so as to ensure proper noise cancellation. To mitigate this matching challenge and relax the required amplifier gains, the sturdy MASH (SMASH) architecture was proposed in [64]. As shown in Fig. 1.14, establishing an encompassing feedback path combining both stages in SMASH, as opposed to having independent feedback loops in MASH, eliminates the need for the digital filters H_1 and H_2. Consequently, the high-gain constraint on the amplifiers, essential for achieving proper matching between the analog and digital components in MASH, is eliminated by SMASH[64]. The resulting transfer function becomes :

$$Y_{out}(z) = STF_1 V_{in}(z) - NTF_1 NTF_2 e_2(z) + NTF_1(1 - STF_2)e_1(z). \tag{1.13}$$

Typically, STF_2 is designed to equal $1 - NTF_2$ in order to ensure that both stage errors are shaped by an identical transfer function. However, this approach no longer completely nullifies the quantization noise of the first stage, thereby affecting SNDR[7]. Although SMASH was initially proposed for DT configurations, CT implementations have also been demonstrated[65, 66, 67]. Noise-cancelling versions have been introduced as well[65, 68, 69],

requiring additional circuit blocks or precise delay matching so as to be able to eliminate the quantization noise of the first stage.

NS-SAR QUANTIZER

Another interesting combination is to incorporate a NS-SAR quantizer within a conventional DT ΔΣ loop, harnessing the low power consumption and compact footprint of the NS-SAR alongside the robustness of the DT ΔΣ architecture. This concept has garnered recent attention, as demonstrated in [70], where a 2nd-order NS-SAR is combined with a 1st-order DT integrator. In [71], the DT loop filter complementing the NS-SAR quantizer serves to increase SNDR and input impedance through an auxiliary impedance boosting technique.

OPTIMIZATION OF HIGH-ORDER SINGLE LOOP MODULATOR

Despite the appeal of the aforementioned multi-loop structures, the current top FOM_{Sc} are in fact achieved using 3rd- or 4th-order single-loop modulators. To ensure sufficient stability performance in such cases, the NTF sharpness is typically designed to be less aggressive than a pure integrator, thereby limiting out-of-band noise gain and enhancing stability. Notably, four of the papers showcasing FOM_{Sc} in excess of 183 dB follow a similar approach : a single-loop modulator with high-efficiency amplifiers in the loop filter. In DT applications, Lee [46] employs a 3rd-order loop with pseudo-pseudo differential ring-amplifier based integrators, resulting in a remarkable FOM_{Sc} of 185.3 dB. Similarly, Liu[47] propose a 4th-order structure featuring a cascoded floating inverter amplifier (FIA). In CT scenarios, Mondal[45] introduces a 3-stack operational transconductance amplifier (OTA) to mitigate noise and enhance transconductance within a 3rd-order modulator. Conversely, Lo[44] presents an energy-efficient power domain shift, reducing the supply voltage from 1.8 V to 1 V within

a two-stage OTA serving as the loop filter amplifier in a 3rd-order modulator. Chandrakumar's CT design [42] is also a single loop 3rd-order modulator, but differs in that the loop filter is modified with an additional gain stage before the first integrator to reduce the power consumed by the input resistor of the RC integrator, thus yielding a FOM_{Sc} of 184 dB.

FEEDFORWARD LOOP STRUCTURE

The most common loop topologies in recent literature include feedforward, which helps reduce voltage swing inside the loop filter, thereby minimizing distortion and easing design constraints for the amplifiers. Recent implementations relying on this approach include [72] which incorporates digital feedforward extrapolation inside a time interleaved structure to reduce hardware overhead. Additionally, [73] proposes a modification to the usual CIFF structure that eliminates the internal feedforward, thus relaxing the requirements of the feedforward summing node.

CONTINUOUS-TIME LOOP FILTER

The classical implementation of the CT loop filter is based on an active RC integrator. However, designing high-precision modulators imposes stringent noise and linearity requirements, resulting in significant power dissipation in this scenario. To address this issue, [74] proposes the addition of a large capacitor at the amplifier input, creating a passive low-pass filter stage before the integrator. This configuration relaxes the transconductance and swing requirements of the amplifier while converting the parasitic pole into a beneficial noise-shaping one. A different approach combines passive and active stages to reduce the number of power-hungry active integrators. In [75], this method uses two op-amps for a 4th-order modulator.

The negative-R assisted integrator[76] is another solution to reduce power consumption of the active RC integrator. Illustrated in Fig. 1.15, this method adds an extra negative resistor input path to the integrator's amplifier realized with an active G_m stage. This integrator structure compensates for finite gain by rendering the virtual ground ideal, thereby relaxing the DC gain, bandwidth, noise, and linearity requirements of the amplifier. This technique is reused in [77] and [78], achieving a state-of-the-art FOM_{Sc} of 181.9 dB in the latter instance.

Another design technique for CT loop filters is using a G_mC integrator cell instead of an active RC integrator. The open-loop transconductance lowers power consumption, although the absence of negative feedback limits circuit linearity. Therefore, a linearization technique introduced in [79] and improved in [80] sets the feedback DAC to have the same nonlinear transfer characteristic as the open-loop transconductance. The combination of both circuit blocks thus allows for cancellation of the nonlinearities.

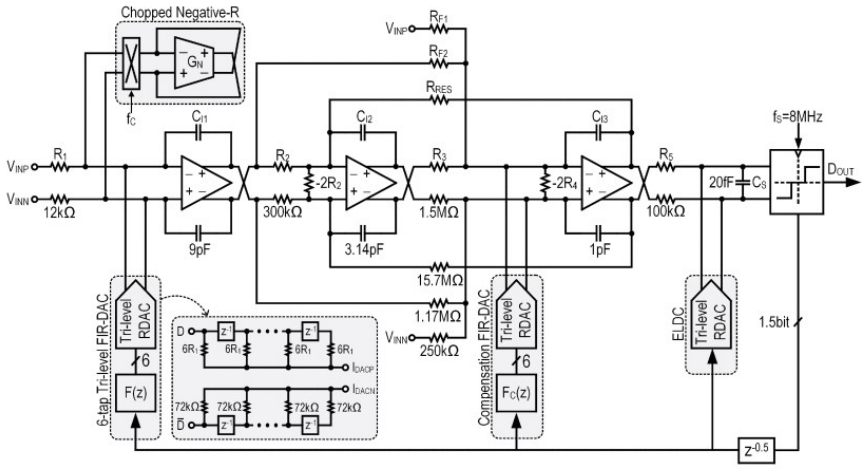

FIGURE 1.15 : Continuous-time ΔΣ modulator with a negative-R assisted first integrator. Reprinted from [78], © 2021 IEEE.

Lastly, the design in [81] combines both filter structures to leverage their advantages : RC integrator for its high linearity, in the most critical first integration stage, and G_mC cells for their high power efficiency, in the subsequent stages.

ALIAS REJECTION

Alias rejection is another interesting property of CT ΔΣ modulators. Recent work[82] proposes a reference-switched resistive feedback DAC to maximise this effect, achieving intrinsic anti-aliasing filtration in excess of 80 dB.

1.7.2 DESIGN TRENDS IN THE INCREMENTAL ΔΣ MODULATOR

MULTI-STAGE CONFIGURATIONS

Recent advancements in ADC design have introduced several improvements to the typical incremental ΔΣ ADC architecture, particularly in multi-stage configurations. One notable configuration is the extended-counting ADC. In this setup, the first stage consists of an incremental ΔΣ ADC, followed by a Nyquist ADC as the second stage [7] as presented in Fig. 1.16. The unique feature of the extended-counting ADC lies in the readily available total error of the first stage, which, through a feedforward structure, becomes accessible at the output of the last integrator of the loop filter. This total error can then be sent to a Nyquist rate ADC, while the output of the first stage is processed by the decimation filter, allowing for complete pipelined operation[83, 84]. By digitizing the error and subtracting it from the output of the decimation filter, accuracy can be significantly improved. Recent works leveraging this technique include [85], where the first stage comprises a 1st-order, 1-bit incremental ΔΣ ADC extended with a 10-bit SAR reusing the same quantizer and employing a serial two-capacitor

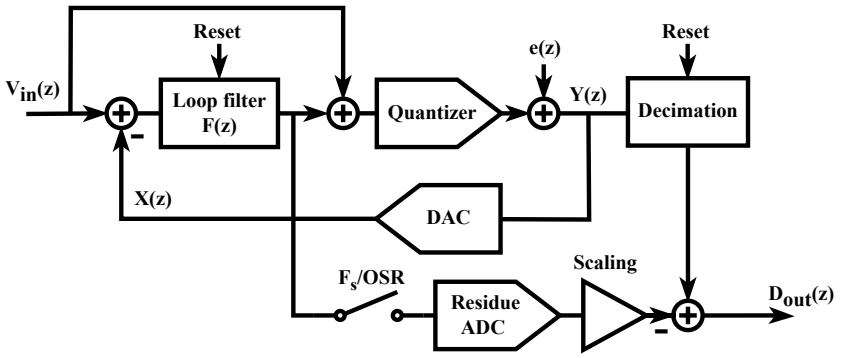

FIGURE 1.16 : Block diagram of the extended-counting ADC.

DAC. In [86], a three-phase variant reusing the same asynchronous SAR quantizer for each stage, with a power efficient capacitor scaling technique, is presented. Other closely related multi-stage structures explored in recent research include the sturdy MASH [87] and the robust MASH [88]. Additionally, three-stage topologies are introduced in [89], tailored for class-D amplifiers, and more recently in [53], featuring a fifth-order configuration where the first two stages are reconfigured to form the third stage in a hardware-efficient manner.

MULTI-PHASE FILTERING

Another interesting technique is to use a multi-phase loop filter able to adjust the properties of the loop filter for different subsets of samples during a conversion. An example involves using slice-based integrators in parallel to optimise the noise/power consumption trade-off [90, 91]. The technique, shown in Fig. 1.17, consists in disabling some integrator slices as the conversion progresses. The noise of the slice-based integrator increases as some slices are disabled but the contribution of the last samples to the output result holds lower weight. Hence, power consumption can be optimised by gradually relaxing the noise constraints with minimal impact on precision.

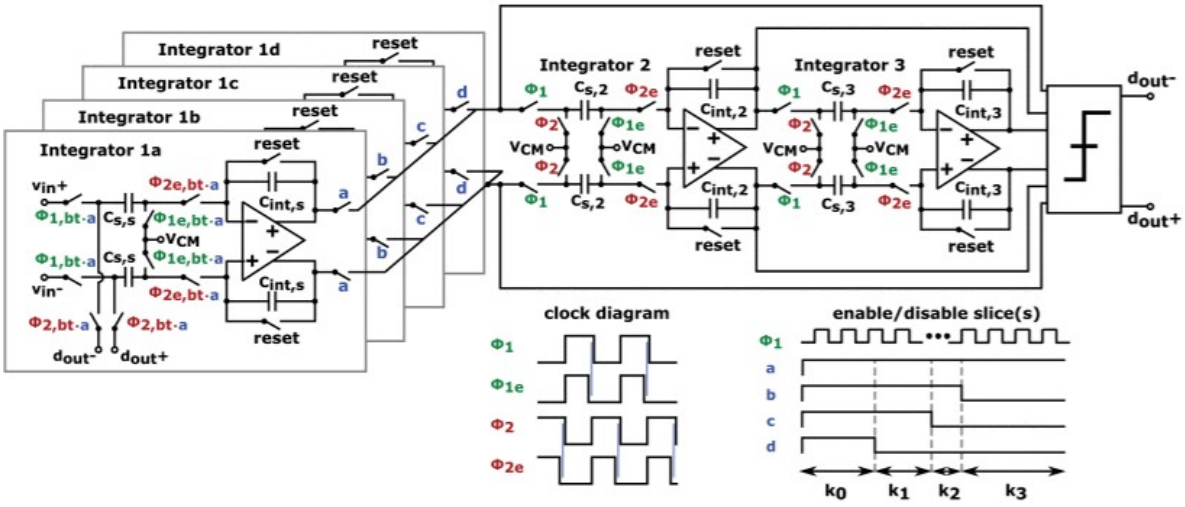

FIGURE 1.17 : Incremental ΔΣ modulator implementing the slice-based integrator. Reprinted from [90], © 2019 IEEE.

Another technique, explored in [92], is to switch the modulator from a 1st-order linear mode to an exponential mode to harness both the benefits of thermal noise suppression in the linear mode and high SQNR in the exponential mode. This design achieves the highest FOM_{Sc} among the reviewed incremental ADC excluding incremental zoom topology, reaching 176.4 dB. The idea is further explored in [93], including frequency domain analysis.

1.7.3 DESIGN TRENDS IN THE NOISE-SHAPING SAR TOPOLOGY

CASCADING LOOP FILTERS

The NS-SAR stands out as a remarkably power- and area-efficient topology. However, achieving a high SNDR poses a challenge due to the topology's high sensitivity to loop filter coefficients, particularly in the simpler yet more efficient EF configuration. The practice of cascading loop filters to attain higher-order noise shaping, which is necessary to strive for high

SNDR, imposes strenuous matching constraints. To address this, [94] proposes a method for cascading loop filters in a nested manner, thus relaxing matching constraints. This approach has been leveraged in numerous designs, yielding impressive performance. For instance, in [95], cascading a 1st-order stage four times yields a FOM_{Sc} of 182 dB.

Expanding upon this concept, [30] proposes nesting both EF and CIFF feedback paths together. This innovation enables the realization of a 3rd-order loop filter using a single amplifier by merging the residue extraction for both feedback paths, thereby simplifying circuitry and reducing power consumption. The combined use of CIFF and EF structures also leverages their respective advantages : the robustness of the CIFF path reduces NTF sensitivity to amplifier gain variations, while the simplicity of the EF path is maintained. The overall design achieves state-of-the-art performance with a FOM_{Sc} of 182 dB.

CAPACITOR STACKING

Another crucial development facilitating the robust order extension technique introduced in the previous section is the capacitor stacking technique. Prevalent in many cutting-edge designs, the capacitor stacking technique was first implemented by [96] as illustrated in Fig. 1.18. This approach utilizes switching capacitors in series with the signal path as summing elements. While capacitor stacking can enhance the power efficiency of EF structures, as shown in [97], its major impact lies in optimizing CIFF structures. By incorporating a series capacitor at the comparator input, the need for multi-input comparators is eliminated. This innovation is particularly beneficial because multi-input comparators are inherently inefficient, contributing to increased thermal noise and power consumption.

The surveyed CIFF NS-SAR designs clearly demonstrate the effectiveness of capacitor stacking over multi-input comparators. For example, [98] and [99] both present 2nd-order

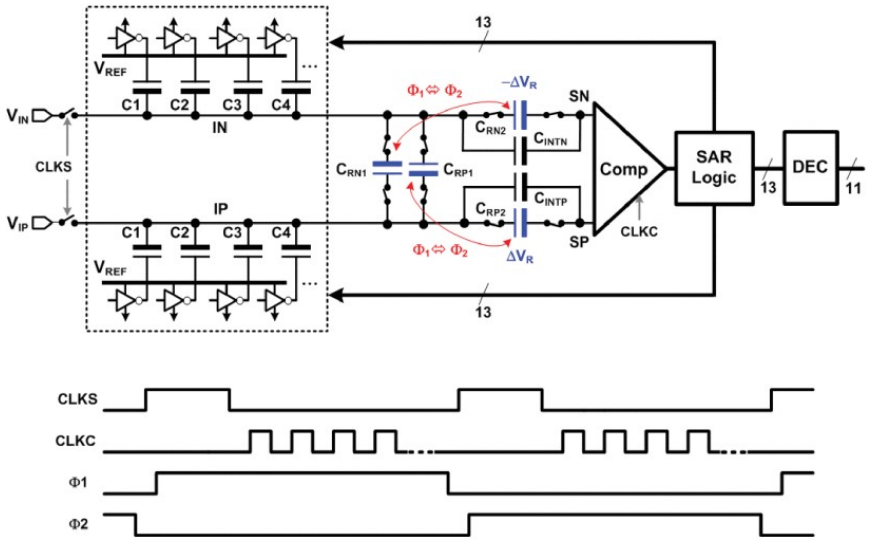

FIGURE 1.18 : Noise-shaping SAR ADC with the capacitor stacking technique. Reprinted from [96], © 2019 IEEE.

CIFF designs with multi-input comparators achieving a FOM_{Sc} of 171 dB, whereas, in contrast, [100] and [101] showcase comparable 2nd-order capacitor stacking-based designs reaching FOM_{Sc} of 179.4 dB and 181.5 dB, respectively.

Capacitor stacking is also applied in fully passive NS-SAR designs as a summing element with four times amplification, achieving FOM_{Sc} of 178.2 dB in [102] and 182.2 dB in [40]. Additionally, Cheng [43] presents the NS-SAR design with the highest FOM_{Sc} of 184.3 dB, featuring a 4th-order CIFF alternating both passive and active integrators with capacitor stacking.

OTHER DESIGN TRENDS

Recently, a CT NS-SAR was proposed for the first time in [103], capitalizing on the power efficiency and anti-aliasing properties of the CT ΔΣ. It addresses the timing conflict

between the CT integral and the DT SAR quantizer by duty cycling the integrator, allocating 5% of the clock period to SAR quantization, with negligible influence on noise shaping performance.

Additionally, Xie [39] introduces an innovative error feedback-cascaded resonator feed-forward (EF-CRFF) topology, enabling NTF optimization through zeros placement, resulting in an impressive FOM_{Sc} of 182.4 dB at OSR of only 5.

Designs aiming to enhance performance and robustness by combining the EF and the CIFF structure are presented in [37, 104]. In [57], the same idea is applied to a MASH configuration.

Finally, [58] proposes the use of two low-resolution pipelined NS-SAR stages with a high interstage gain (ISG) of 16 to achieve high SNDR while reusing the same amplifier for filtering and ISG.

1.7.4 DESIGN TRENDS IN THE ZOOM TOPOLOGY

DYNAMIC ZOOM

In the original zoom topology, the coarse quantization defining the zoomed range of the DAC is performed sequentially with the fine ΔΣ stage. This operation in succession severely constrains the bandwidth of the zoom ADC. For instance, initial designs by Souri and Makinawa are capped at 10 S/s [31] and 25 S/s [32]. To address this issue, the dynamic zoom is proposed [105], which involves running both stages concurrently, in parallel. This approach also enables the use of a free-running ΔΣ as the fine stage. Nevertheless, parallelizing both stages introduces a delay before the zoom reference can be updated due to the limited conversion speed of the coarse quantizer. If the input varies rapidly, it may surpass the zoomed

range, pushing the modulator beyond its stable bounds. To mitigate this possibility, over-ranging can be used, whereby the zoomed range is enlarged to ±k levels from the coarse quantizer output. This expanded range reduces the risk of being overrun by the input signal. The design in [105] uses this technique to achieve a bandwidth of 20 kHz, sufficient for audio applications. However, the DAC reference level is updated only once every 5 cycles, rendering it vulnerable to out-of-band interferers. The dynamic zoom technique in [50] addresses this issue by refreshing the reference concurrently every clock cycle using an asynchronous SAR coarse quantizer. This faster reference update allows for lower swing and enhanced power efficiency, thereby leading to a state-of-the-art FOM_{Sc} of 183.6 dB at 1 kHz bandwidth.

"FUZZ" MITIGATION

Another challenge with zoom ADC is the introduction of out-of-band "fuzz" in the output spectrum, which degrades SNDR [50]. This issue arises from the summation of the outputs of the coarse and fine stages in the digital domain. This digital summation assumes that the STF of the fine ADC is exactly unity, which is not always the case, especially at higher frequencies for CIFF ΔΣ presenting STF peaking [50]. The digital summation then becomes non-ideal, introducing quantization error leakage from the coarse stage into the output. In [50], this problem is addressed with a digital filter replicating the STF at the digital output of the coarse stage, akin to a MASH architecture. Eland [48] proposes the use of an analog residue feedforward path to ensure a unity STF, significantly reducing the fuzz issue. With a 2-bit quantizer, this allows for a 40% OSR reduction, resulting in a state-of-the-art FOM_{Sc} of 183.1dB. The modulator with the additional feedforward path is shown in Fig. 1.19. Recently, this concept has been revisited in [106] with a fully dynamic zoom using FIA achieving sub 1 μW power consumption and a FOM_{Sc} of 182.2 dB.

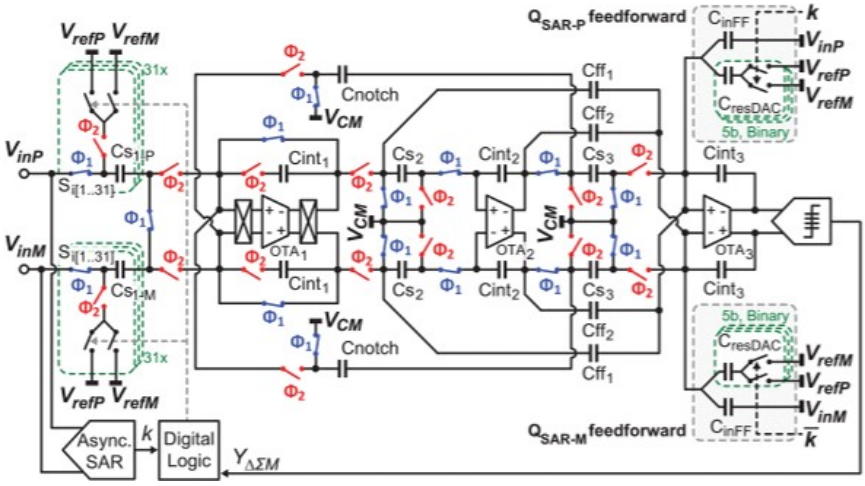

FIGURE 1.19 : Dynamic zoom ADC with analog feedforward path reducing the fuzz issue. Reprinted from [48], © 2021 IEEE.

CONTINUOUS-TIME ZOOM

The advent of dynamic zoom with a free-running ΔΣ fine stage also facilitated the introduction of CT zoom ADC, which aim to leverage the efficient loop filter amplifier and easy drivability properties of the CT ΔΣ architecture [107]. Still, special care must be taken in designing the feedback DAC and the chopping circuitry necessary to suppress 1/f noise. Indeed, CT ΔΣ are more sensitive to DAC waveform non-idealities and chopping artifacts than their DT equivalent. In [107], a novel intersymbol interference (ISI) reduction technique based on matched layout in its DAC and a pseudo-differential inverter-based amplifier are employed, achieving FOM_{Sc} of 181.5 dB at 20 kHz.

Recent works propose using oversampling ADC as coarse quantization stages in CT zoom architectures, with [108] using a NS-SAR and [109] employing a CT ΔΣ modulator. This configuration allows the shaping of the fuzz error of the coarse quantizer, improving SNDR and achieving FOM_{Sc} above 180 dB in both cases. Finally, a highly area-efficient

hardware-reusing zoom-incremental-counting ADC with CT ΔΣ fine stage is presented in [110].

OTHER DESIGN TRENDS

Among the surveyed works, one recent approach uses FIA-assisted residue extraction, allowing the NS-SAR fine stage to skip 75% of the sampling operations. Combined with a lower OSR, the design reaches a bandwidth of 150 kHz, the fastest in all the assessed zoom topologies [111]. In [112], a self-timed dynamic amplifier-based zoom ADC is introduced that eliminates the need for power-hungry high-frequency clock generation. In [113], an adaptable pole-optimization technique mitigates the performance degradation normally associated with scaling resolution/bandwidth. Furthermore, [114] presents the first pseudo-pseudo-differential incremental zoom design. It employs simple single-ended circuitry to process differential inputs, with a three-phase technique to reduce common-mode noise leakage, resulting in great performance with a FOM_{Sc} of 180.8 dB.

AN ALTERNATIVE TO THE ZOOM TOPOLOGY : THE NESTED ΔΣ MODULATOR

A novel approach, distinct from traditional zoom ADC architectures but targeting the same key challenges, is the nested ΔΣ modulator introduced by Guo in [49]. This architecture comprises an inner analog ΔΣ modulator embedded within an outer analog-digital ΔΣ modulator as illustrated in Fig.1.20. The swing of the inner ΔΣ is suppressed by the outer loop, enabling the same low-power benefits as in the zoom ADC. However, unlike zoom ADC, the nested structure suffers neither from distortion nor from fuzz leakage by virtue of its different loop construction. This architecture surpasses most conventional zoom ADC, achieving a remarkable FOM_{Sc} of 183.5 dB at a 10 kHz bandwidth as well as SNDR of 109.2 dB.

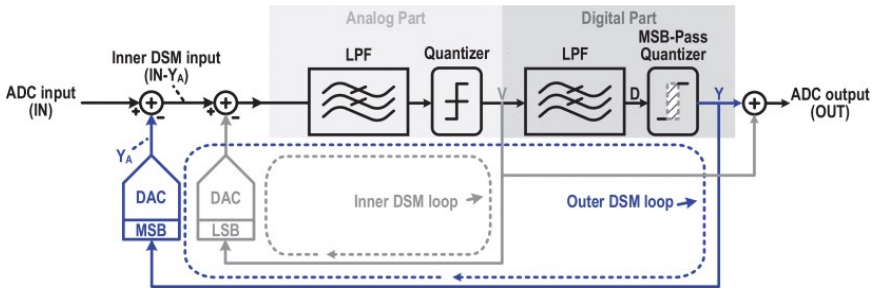

FIGURE 1.20 : Architecture of the nested ΔΣ Modulator. Reprinted from[49], © 2023 IEEE.

1.7.5 DESIGN TRENDS IN THE TIME-DOMAIN ΔΣ MODULATOR

VCO-COUNTER ARCHITECTURE

The first generation of oversampling ADC designs making use of TD signal processing is the VCO-counter architecture[115, 116], wherein a VCO performs voltage-to-frequency conversion, and a reset counter provides a digital output proportional to frequency, as depicted in Fig. 1.21. In this structure, neither feedback nor an integrator is needed. Noise shaping is achieved through the summation of the rising edges at the output of the VCO inside the counter, enacting intrinsic integration. The absence of a feedback path significantly reduces design constraints by eliminating the need for a DAC and its associated linearity and precision challenges. Recent designs leveraging this open-loop oversampling concept include [117], in which a current-controlled oscillator (CCO) with a variable nominal frequency manages to improve power efficiency, and [118], in which a PWM-based voltage-to-time converter

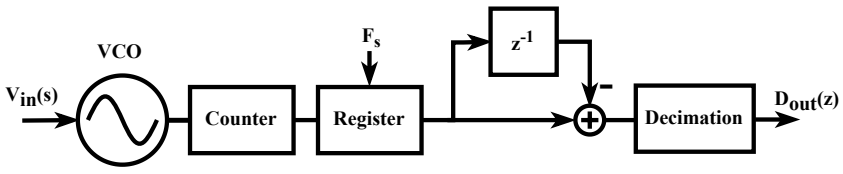

FIGURE 1.21 : Block diagram of a simple implementation of the VCO-counter oversampling ADC.

precedes the VCO so as to enhance input impedance and linearity, achieving SNDR above 80 dB while consuming only 2.2 μW.

CONTINUOUS-TIME FILTER

A structure introduced in the late 1990s[120] added feedback and a CT integrator upstream of the VCO quantizer, similar to those found in CT $\Delta\Sigma$ modulators. This structural change allows for greater flexibility in loop filter and noise-shaping design. Many recent state-of-the-art designs adopt this structure. Notably, [119] features a capacitive-π network that makes the CDAC independent from the load capacitance of the integrator, thereby reducing capacitor footprint and power consumption. The technique is illustrated in Fig. 1.22, where

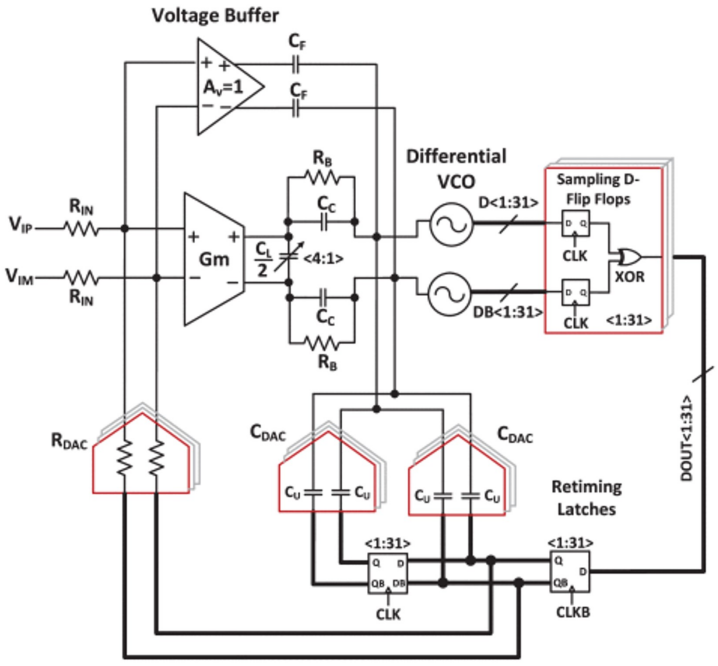

FIGURE 1.22 : Time-domain $\Delta\Sigma$ modulator with VCO quantizer and G_mC integrator. Reprinted from[119], © 2021 IEEE.

the π network is formed of C_L, C_C and C_{DAC} at the output of the G_m stage. The design in [121] improves upon this approach by utilizing a resistive feedback DAC in parallel with the degeneration resistance of the first G_m stage to improve linearity of the system.

FULLY TIME-DOMAIN ARCHITECTURE

One drawback of the aforementioned TD architectures is the need for the loop filter to include an active G_m stage. Consequently, part of the signal chain is processed in the voltage domain, which remains subject to limitations in advanced technology nodes with reduced supply voltages. Hence, OTA-less designs have been proposed that use passive RC networks for the loop filter [122]. Other designs employ techniques involving VCO, CCO, and phase detectors to construct analog filters, as explained in [123]. These designs include some of the most efficient and precise TD $\Delta\Sigma$ ADC. For example, the design in [124] introduces a new feedforward structure in a 3rd-order modulator, linearizing the VCO and achieving the highest SNDR in TD $\Delta\Sigma$ of 92 dB with a FOM_{Sc} of 179.1 dB. Furthermore, this highly digital topology, where both quantizer and loop filter are VCO-based, allows for effective layout automation. Zhong's design [125] is fully synthesized and achieves the best FOM_{Sc} for a TD $\Delta\Sigma$ ADC at 180.1 dB. Another fully digital structure is presented in [126], where the loop structure is based on a digital phase-locked loop (PLL) incorporating an array of phase frequency detectors to reduce the VCO center frequency and, consequently, minimize power consumption.

MULTI-STAGE ARCHITECTURE

Multi-stage structures are also prevalent, where one or both of the stages is implemented in TD. TD designs where one of the stages still operates in the voltage domain are deemed

hybrid in Fig. 1.11. Employing a TD second stage offers undeniable advantages : the noise shaping from the prior stage and the minimal swing of the quantization error help linearize the VCO without necessitating additional design tricks. Recent work, such as that in [62] and [61], has delved into MASH structures with both stages implemented in TD. MASH structures combining a DT ΔΣ [60] or a NS-SAR [59] first stage with a VCO-based second stage have also been explored. Furthermore, combinations featuring power-efficient NS-SAR structures have been presented, such as in [127], where a VCO integrator supplements a 2nd-order NS-SAR with an anti-aliasing filter based time-to-voltage conversion between both sections. Finally, the design outlined in [128] integrates a TD comparator within a NS-SAR structure for superior thermal noise performance.

AN ALTERNATIVE HYBRID APPROACH : HSIEH'S DESIGN

Among all oversampling ADC designs covered in this survey, Hsieh's topology [41] achieves both the highest FOM_{Sc} and FOM_{Wa} at 186.8 dB and 0.6 fJ/conv-step, respectively. The topology, shown in Fig. 1.23 consists of two Nyquist SAR quantizers forming the first stage, each handling half of the input swing so as to effectively double the allowable input range. To minimize power consumption, two main techniques are employed. First, the unused of the two quantizers is set to idle mode since each one is responsible for handling a distinct portion of the input range. Second, a low supply voltage of 0.4 V is used.

To enhance SNDR at minimal power overhead, a second stage 1st-order TD incremental ΔΣ reuses as much of the same circuit components as possible. A voltage-controlled delay line (VCDL) within the SAR first stage is reconfigured into a VCO integrator to process the residue error readily available on the SAR CDAC array. After combination of the output of the two successive stages by the digital backend, a SQNR improvement of 24 dB is achieved compared

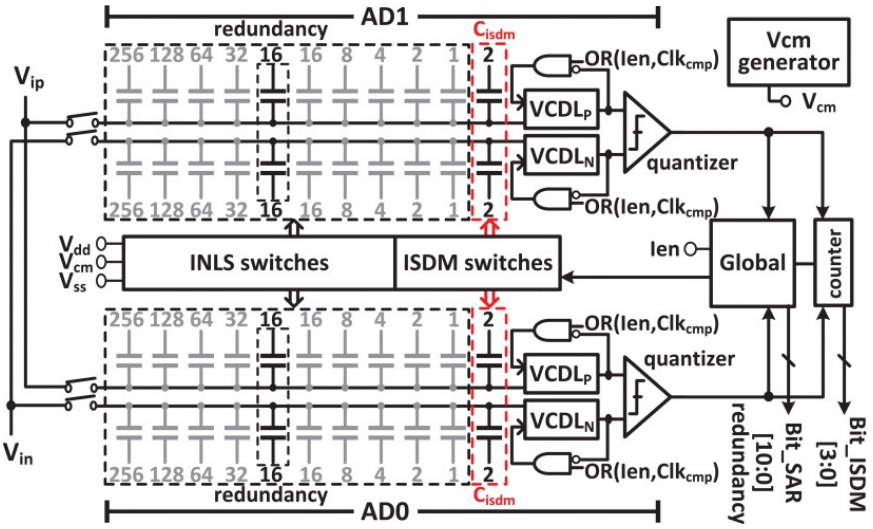

FIGURE 1.23 : Architecture of the design achieving the highest FOM. Reprinted from[41], © 2019 IEEE.

to the SAR first stage only. The overall design operates with a bandwidth of 135 kHz and a power consumption of just 0.6 μW.

1.8 CIRCUIT-LEVEL DESIGN TRENDS

1.8.1 AMPLIFIER AND LOOP FILTER DESIGN TRENDS

One of the most critical circuit blocks in $\Delta\Sigma$ modulator design is the loop filter along with its amplifiers. If not designed carefully, distortion and thermal noise caused by the amplifier may significantly degrade the performance of the entire ADC. As for insufficient DC gain, it may result in non-ideal integration, negatively affecting noise shaping and SQNR. Also, insufficient bandwidth can cause settling errors, severely limiting system accuracy. Finally, the amplifier often consumes a significant portion of the power budget of a $\Delta\Sigma$ ADC. For all these reasons, developing amplifier structures to offer more favorable design trade-offs remains a significant research focus.

CONVENTIONAL AMPLIFIER

The traditional Miller compensated amplifier is seldom used in recent designs [53, 75]. Instead, designers often prefer single-stage telescopic cascode [60, 92], folded cascode [73, 90, 91], or gain-boosted cascode [72, 80, 86] amplifiers, which offer better power efficiency at the expense of output swing. Another noteworthy amplifier topology for CT ΔΣ modulators is the feedforward compensated OTA. This topology provides higher bandwidth for the same power consumption as a Miller compensated amplifier but introduces more swing in the transient response due to an additional zero in the transfer function [7]. This makes the technique harder to implement in settling-based DT modulators because the additional transient swing needs to settle completely. However, the technique is well suited for CT modulators where the entire waveform is relevant and slowly settling transients don't really matter. Many CT designs make use of this technique to enhance power efficiency [56, 82, 87, 129, 130, 131], including some of the highest FOM_{Sc} recorded [44, 45].

INVERTER-BASED AMPLIFIER

The inverter-based, or current-reuse, amplifier was introduced in ΔΣ modulators by Chae [132]. These amplifiers consist of an inverter biased at the center point, which can be used either as the complete amplifier or as an input stage. This design effectively doubles transconductance since both PMOS and NMOS transistors are active simultaneously and contribute to overall transconductance. This improves power efficiency because higher transconductance can be reached for the same bias current. However, this topology is more sensitive to PVT variations and parasitic impedance. Recent designs featuring inverters as amplifiers are presented in [71, 77, 103, 133, 134]. To achieve higher DC gain, some authors use a current-reuse first stage, within a two-stage OTA [100] or in a cascode structure [48, 50, 74, 107, 113, 135]. A

self-bias cascode structure, introduced in [114], reduces power consumption from the bias circuitry.

RING AMPLIFIER

The ring amplifier [136] is an innovative amplifier topology that uses a ring oscillator with a dead zone integrated into a feedback loop. The dead zone forms a range where the ring oscillator's output does not change, forcing the output to settle at a fixed value. The advantages of this topology include inherent rail-to-rail output, high slew rate, and excellent scaling with technology nodes. However, there exists a fundamental trade-off between robustness and precision, dictated by the size of the dead zone. Two designs by Lee [46, 54] use this technique in the surveyed state-of-the-art, with [46] achieving the second-best recorded FOM_{Sc} at 185.3 dB.

BUFFER-BASED AND PASSIVE LOOP FILTERS

The source follower integrator [69, 137], illustrated in Fig. 1.24, is an example of an integrator topology that simplifies design, as it requires only a buffer, a few switches, and capacitors. Many designs also opt for passive filtering using RC or passive switched-capacitor networks as loop filters [59, 99, 122, 138]. The drawback of using passive or buffer-based circuitry is that the integration performed by the circuit is non-ideal, which reduces the effectiveness of the noise shaping.

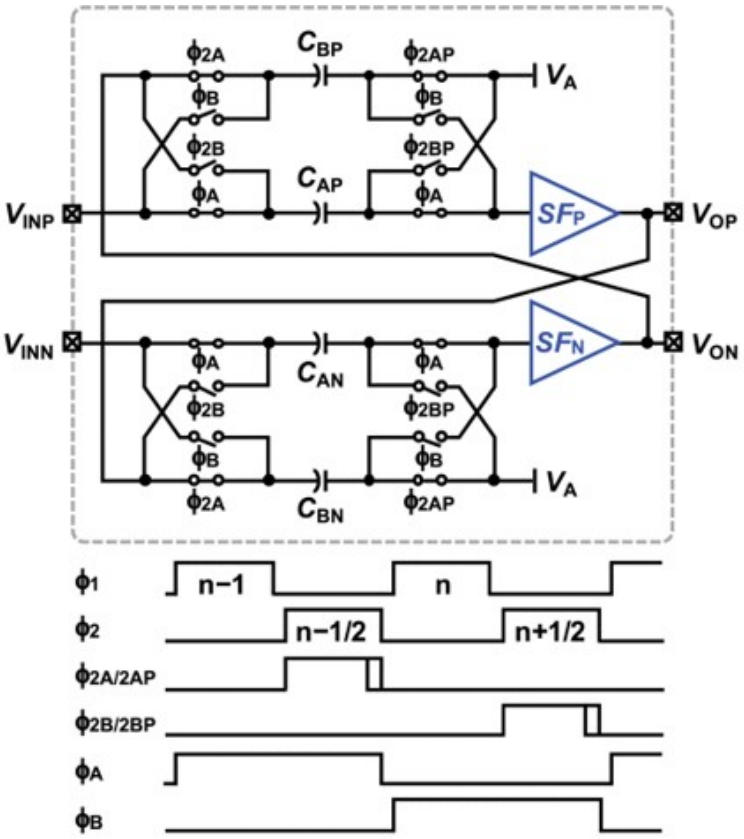

FIGURE 1.24 : Schematic and timing diagram of the source follower integrator. Reprinted from[69], © 2018 IEEE.

DYNAMIC AMPLIFIER

Dynamic amplifiers are highly popular in recent state-of-the-art designs, as they have the potential to curb the high static power consumption associated with conventional amplifiers. By having its biasing current vary during operation, a dynamic amplifier improves power efficiency as it draws high current only when necessary and limits it during idle periods. Like the ring amplifier, the dynamic amplifier must be used in a settling-based circuit, such as the switched-capacitor integrator of a DT ΔΣ modulator, to be able to reset the bias current variation effectively.

The concept of a variable bias current amplifier was first proposed around 1980 [139, 140, 141]. Its application in modern ADC design was revisited by Chiang [142] in the form of a charge-steering amplifier for pipeline ADC. The operating principle involves precharging capacitors at the output of a differential pair. During amplification, the charges on both pre-charged capacitors discharge at a rate proportional to the differential input, thereby generating amplification, as shown is Fig. 1.25. This idea has been adapted to be used in oversampling ADC [29, 98, 143], notably in Liu's NS-SAR design [38], to help achieve a FOM_{Sc} of 180.1 dB and a FOM_{Wa} of 5.8 fJ/conv-step.

Despite its impressive performance, the charge-steering amplifier has a variable common mode at the output and is sensitive to PVT variations, which makes calibration crucial, as demonstrated in [142]. To address these issues, the floating inverter amplifier (FIA) was first proposed for use in a NS-SAR design by Tang in 2020 [101]. The amplifier, depicted in

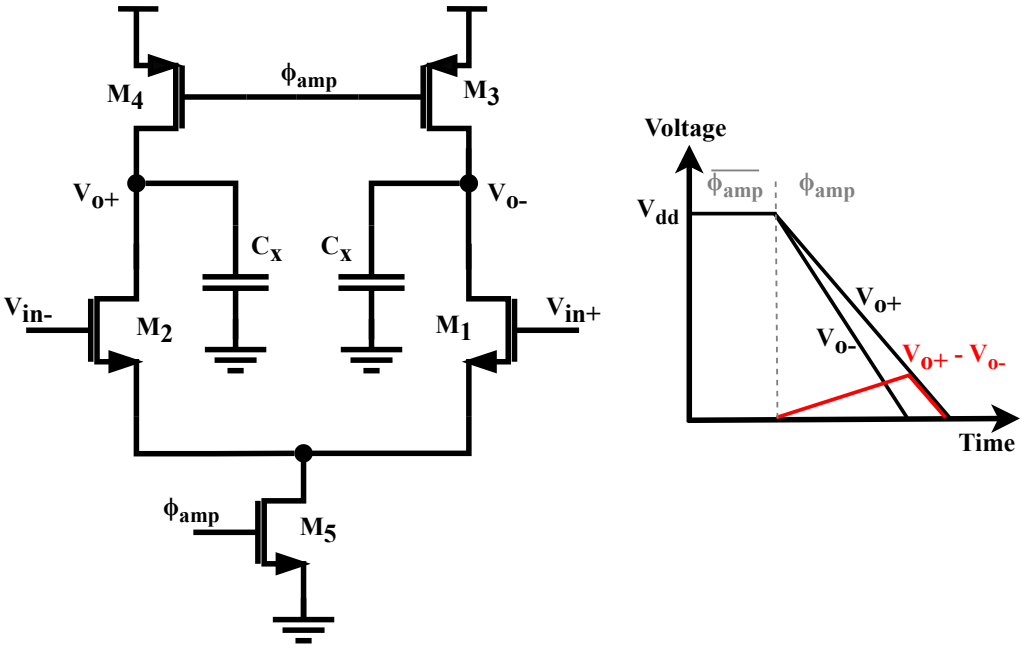

FIGURE 1.25 : Schematic of the charge-steering dynamic amplifier and its simplified output waveforms.

Fig. 1.26, consists of two inverters operating as a differential amplifier. A large reservoir capacitor is precharged and used as the power supply during amplification, allowing for floating operation, which directly solves the varying common mode and PVT sensitivity issues of the previous dynamic amplifier design. The initial NS-SAR design of [101] includes a two-stage FIA that achieves ideal 2nd-order noise shaping at low power consumption, reaching a FOM_{Sc} of 181.5 dB.

Many recent designs have adopted and improved upon this amplifier structure, achieving state-of-the-art FOM_{Sc} in excess of 180 dB, such as [30, 43, 47, 106, 111]. Two key improvements are the use of correlated level shifting and dynamic body biasing, as proposed in [52], which enhance gain and swing while improving transconductance at the end of the amplifica-

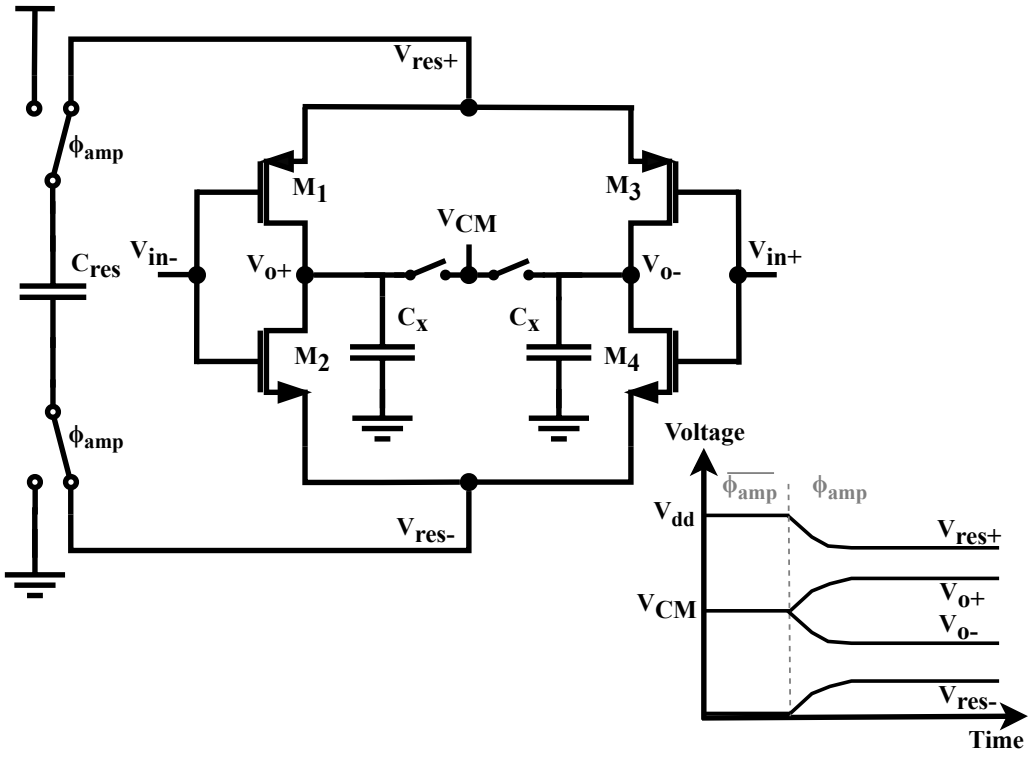

FIGURE 1.26 : Schematic of the floating inverter dynamic amplifier and its simplified waveforms.

tion phase when the reservoir capacitor is nearly empty. Another significant enhancement is the introduction of an additional operation phase for thermal noise cancellation, as seen in [144]. Also, a dynamic biasing technique incorporating the swing-enhanced FIA is discussed in [145, 146]. Tang also presents further improvements to his original design in [147]. Other designs using the FIA include [39, 57, 70, 112, 128, 148].

An extension of the dynamic amplifier concept involves altering different amplifier properties dynamically during the amplification phase. For instance, in [149], the concept of incomplete settling[150] is leveraged in a duty-cycled amplifier to control the circuit's gain. The final implementation also includes a power efficient switched biasing circuit. In [94], a multiphase settling technique is introduced that toggles an output resistor on and off during amplification. This method enables a better balance between noise, gain sensitivity, and power efficiency. Similarly, in [55], a segmented integration technique is employed to achieve the same goal. This approach uses two different amplifiers : first, a high slew rate inverter-based amplifier, followed by a low-noise differential pair to complete the integration.

1.8.2 NOISE MITIGATION TRENDS

Most oversampling ADC designs are limited by thermal noise, i.e. the majority of the noise budget is allocated to thermal noise, with quantization noise kept relatively small. This approach is preferable for power efficiency because reducing quantization noise requires less power compared to reducing kT/C noise, which would involve using large capacitors, thereby heavily loading amplifiers and driving circuits. Consequently, circuit design techniques that can help reduce thermal noise efficiently, aside from resorting to large capacitors, are highly sought after for improving SNR at low power.

FLICKER NOISE

Flicker noise could be a significant noise source if not addressed properly. However, since it is confined to low frequencies, it can be effectively managed using well-established offset-cancellation techniques such as chopping [151] and auto-zeroing [152]. In CT ΔΣ modulators, however, chopping tends to introduce quantization noise aliasing into the signal, degrading performance [153]. This issue is addressed in [154], where a chopping artifact rejection technique is introduced by setting the chopping frequency to match the sampling frequency.

NOISE CANCELLATION

A common approach to reduce thermal noise in circuits is to use noise cancellation [155]. The principle of operation involves sampling the kT/C noise on a capacitor, then subtracting it from the signal path during circuit operation via a switched-capacitor network. Multiple variations of this approach are used in recent oversampling ADC design [30, 57, 144, 156, 157].

For instance, in [144], an additional phase is added to the FIA to allow sampling noise cancellation (SNC), as shown in Fig. 1.27. The additional capacitors C_{SNC} and switches used for SNC are shown in red. At the end of the sampling phase, the FIA is activated to sample the amplified input change with the sampling noise on C_{SNC}. When the sampling phase ends, the charge transfer begins for both the main sampling capacitor C_S and C_{SNC}. The sampling noise stored on both of these capacitors cancels itself when the charges are transferred to the integrating capacitor C_I. The capacitor ratio between C_S and C_{SNC} must match the amplifier gain for perfect noise cancellation during charge transfer. Hence, some smaller residual thermal noise is expected with the inevitable process mismatches. The thermal noise introduced by the

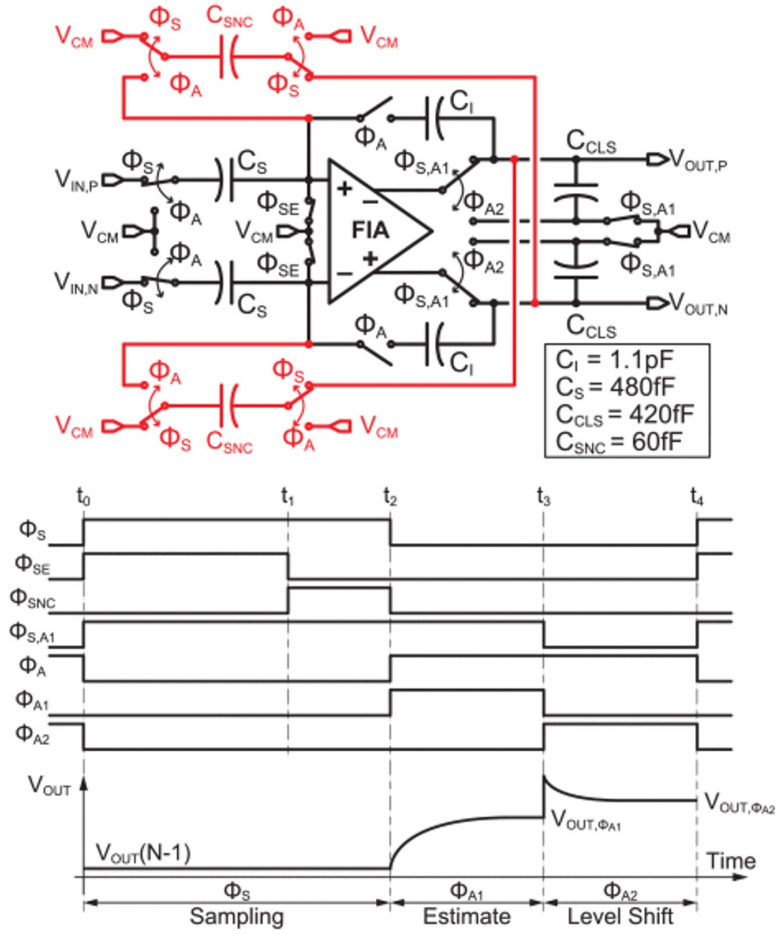

FIGURE 1.27 : Noise cancellation circuit inside a FIA-based loop filter with timing diagram. Reprinted from [144], © 2023 Matsuoka et al., CC BY 4.0.

additional circuitry is reduced by a factor of the amplifier's gain, preventing it from degrading performance.

MAJORITY VOTING

Another technique introduced in [158] to reduce thermal noise in the NS-SAR quantizer is majority voting. The idea is to repeat one or more of the least significant bit (LSB) comparisons multiple times and take the majority output. This allows for a significant reduction

in thermal noise, thus relaxing design constraints. The idea is further optimised in the same work by applying the majority voting technique in a data-dependent manner. The majority voting technique is only applied when the noise is at a critical level for the SAR comparator. Since the impact of noise depends on the input level, a detector circuit determines when noise becomes critical and majority voting should be applied. Otherwise, power is saved by turning off majority voting.

In [159], the same concept is applied, but only to the LSB, using simplified logic and a digital-friendly circuit that doesn't require an error detector. The drawback is a less efficient implementation of the technique. In [99], an improved tri-level majority voting scheme is introduced by exploiting more information from the comparator and providing an extra decision level. Finally, the technique is used with an 8-fold LSB repetition in [40], where the ADC achieves FOM_{Sc} of 182.2 dB.

1.8.3 DAC MISMATCH COMPENSATION DESIGN TRENDS

Mismatch and non-idealities in the feedback DAC are among the most critical limitations of ΔΣ ADC. Since the error correction loop does not shape errors originating in the feedback path, the DAC must be at least as linear as the overall ADC requirements. When high precision is needed, the DAC often becomes the bottleneck because the matching accuracy of the fabrication process is unable to meet the required specifications. Techniques such as laser trimming can be used to improve DAC matching, but at a very significant cost.

CALIBRATION

A widely used solution to address the DAC mismatch issue is digital foreground calibration. Foreground calibration occurs while the ADC is not running, either at start-up or

in periodic breaks during operation. This technique uses a lookup table (LUT) encompassing the nonlinear response of the DAC, in order to correct the modulator output as shown in Fig. 1.28. The LUT can initially be populated by reorganizing the ADC circuit blocks [157, 160, 161], necessitating additional circuitry. Simpler implementations can be realized through the application of a spectrally pure sinusoidal input [162, 163]. However, generating such an input signal on-chip for periodic calibration poses a difficult challenge. To address this conundrum, an alternative implementation using an out-of-band tone was proposed in [164]. An alternative foreground calibration technique is presented in [104] in which a least mean squares filter is used to minimise the impact of quantization noise on mismatch error extraction, simplifying the calibration circuitry and enhancing robustness to process, voltage and temperature variations.

Another approach is the analog calibration of the unit elements of the DAC to improve matching and linearity. An example of this method is presented in [65], where a current-steering DAC has its unit current sources periodically calibrated against a reference, an idea adapted from [165].

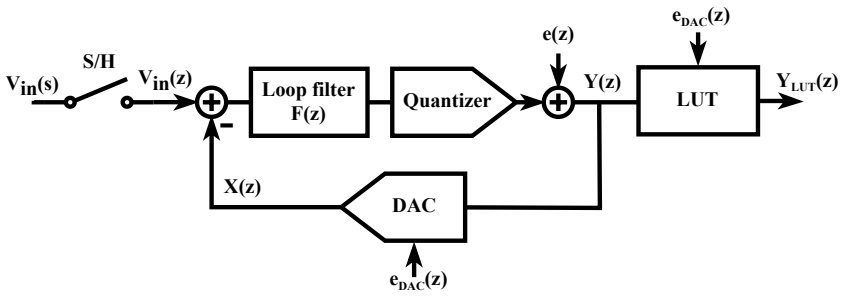

FIGURE 1.28 : Block diagram of the foreground digital calibration of the DAC errors.

INHERENTLY LINEAR DAC

To alleviate the need for additional calibration circuitry, a very simple technique to achieve high linearity in the DAC feedback is to use a 1-bit quantizer and a 1-bit DAC. In a 1-bit modulator, only two quantization levels exist, forcing the system to remain perfectly linear after implementation, regardless of how the quantization levels vary with respect to one another. Several design examples leveraging this property are proposed in [47, 74, 85, 145]. However, a 1-bit system is not without its own limitations : higher quantization noise, reduced maximum stable amplitude of the modulator, and increased sensitivity to jitter and DAC waveforms in CT implementations. To avoid renouncing the benefits of multilevel quantization, inherently linear DAC topologies have been proposed. Notably, a DAC architecture where every element is used for each level generation keeps the output linear even with mismatch, as proposed in a 5-level version in [166] and a 13-level version in [167]. A tri-level inherently linear DAC in a SMASH architecture is also proposed in [87]. Finally, a segmentation technique to improve DAC linearity and achievable SNDR is proposed in [168].

CONTINUOUS-TIME MODULATOR

CT $\Delta\Sigma$ modulators are particularly sensitive to DAC non-idealities because jitter and waveform symmetry also deteriorate the modulator's performance. Consequently, research on DAC mismatch mitigation has accorded importance to this topology. One widely used technique is to insert a FIR filter before the DAC to smooth out sharp transitions. With smaller transition steps, the DAC becomes less sensitive to jitter since any temporal fluctuation causes a smaller voltage error in the integrator. A differential resetting scheme with a FIR filter DAC is introduced in [131] to improve jitter robustness and DAC linearity. The zap-switch technique

is also proposed in [129] with a return-to-open FIR filter DAC to address ISI and transition waveform sensitivity.

MISMATCH ERROR SHAPING

Another elegant technique to address the stringent DAC linearity constraint is mismatch error shaping (MES). MES techniques introduce noise shaping to DAC mismatch and nonlinearity in order to diminish their impact on ADC performance. A straightforward approach to achieving this mismatch noise shaping is to shuffle the DAC unit elements for each sample. Indeed, due to mismatch, each DAC element presents a small error relative to the others. Shuffling the DAC elements averages their weight errors over the multiple samples used in the conversion process, by virtue of the strong low-pass filtering provided by the decimation filter. The simplest and most widely used element shuffling scheme is data weight averaging (DWA) [169]. This technique involves rotating the usage of each DAC element in sequence, analogously to a barrel shifter, resulting in 1st-order mismatch shaping.

A limitation of DWA lies in that the simple rotation of DAC elements is highly deterministic, which inevitably introduces spurs in the output spectrum[7]. To mitigate this issue, other element rotation schemes have been proposed to introduce randomness to the element selection algorithm, limiting the spurs but also MES effectiveness. For instance, bidirectional DWA[170] alternating rotation direction or butterfly shuffling[171], a scheme based on the butterfly operation of the fast Fourier transform (FFT), were proposed. In recent state-of-the-art designs, many top-performing ADC leverage DWA or other element shuffling techniques to improve DAC linearity[42, 44, 46, 48, 50].

DAC element shuffling, while attractively simple, merely provides 1st-order MES. An alternate technique is to add a mismatch error feedback, similar to $\Delta\Sigma$ modulation, to allow

MES by an arbitrary function. Early works proposed vector-based DAC element selection logic, which included mismatch error feedback with filtering[7, 172]. With this method, selecting a higher-order filter enables achieving arbitrarily high-order MES, albeit at the cost of increased circuit complexity. For instance, a second-order implementation is detailed in [173], where the vector element selection logic is realized with a partial sorter within a slightly modified architecture that requires an additional filter. In another work, Sun [174] proposed a novel vector-based MES architecture without the extra filter, enhancing hardware efficiency, MES, and stability performance. More recently, an implementation of vector-based MES in a CT $\Delta\Sigma$ modulator further improves the robustness of Sun's architecture by adding a compensation scheme to the partial sorter [175].

Lately, a similar technique based on subtracting the mismatch error of the previous sample to the current conversion sample to enable 1st-order MES was proposed in [176]. The technique is reused, along with DWA, in [177] to achieve a calibration-free ADC, as the improved linearity from MES is sufficient to meet system requirements. Another design presented in[102] adapts the technique to achieve 2nd-order mismatch shaping[178], reaching SNDR above 90 dB without any calibration.

1.8.4 INPUT SWING OPTIMISATION DESIGN TRENDS

The choice of input swing for an ADC can have a significant impact on the overall performance of the system. Most designs typically make use of the full range of the supplied voltage. However, adjusting the input swing, whether upward or downward, may present notable design trade-offs.

BOOSTING THE INPUT SWING

In the surveyed state-of-the-art designs, only two opted to boost the input swing to a value greater than that of the supply voltage. The rationale for maximizing input swing is to enhance SNR without power overhead or, conversely, to decrease power consumption for a given SNR. By increasing the input swing for the same supply voltage, power efficiency is enhanced because it relaxes the noise constraints for a specific SNR specification, given the higher input signal. This allows for smaller thermal noise mitigation capacitors, reducing amplifier loading and consequently lowering power consumption. In contrast, increasing the supply voltage to achieve a higher input swing is not beneficial, as power consumption rises at the same rate as the increased SNR.

This technique is very effective, as evidenced by the design by Hsieh [41] with the top FOM_{Sc}, as discussed in detail in section 1.7.5. This design is exceptionally power-efficient, featuring a doubled SAR input stage that enables twice the input swing. The other design to boost the input range is Prochet's TD ΔΣ design [124]. It features a CCO-based loop filter with a novel feedforward path that helps linearize the CCO and eliminates the need for an additional DAC. The input swing is increased by raising the DAC reference voltage from the 0.8 V supply to 1.2 V, resulting in a 1.8 V_{pp} differential input swing. The boosted input swing improves SNDR by 2 dB with minimal power penalty, contributing to the design achieving the highest SNDR for a TD ΔΣ at 92 dB.

REDUCING THE INPUT SWING

The main drawback of boosting the input swing is that the ADC becomes more difficult to drive. The input buffer feeding into the ADC must be highly linear to avoid distorting

the input signal, often requiring a supply voltage higher than the desired swing, leading to substantial power consumption. Therefore, keeping the swing low makes the ADC easier to drive, which can simplify input buffer circuitry and save power. An example of a design following this approach is Lim's CT ΔΣ ADC [154]. This design leverages a capacitively coupled instrumentation amplifier (CCIA) as an in-loop input buffer with high input impedance, as illustrated in Fig. 1.29. With its 1.8 V supply, it features a 60 mV_{pp} input swing, which can be directly driven by most sensors. This is highly attractive since additional off-chip input amplifiers could easily exceed the power consumption of the entire ADC.

Another design, described in [121], presents a 300 mV_{pp} input swing in a 1 V supply ADC. Here, the design utilizes a TD quantizer with a G_mC loop filter. The G_m amplifier is used directly as the input, providing a high impedance, easy-to-drive terminal. Linearity is improved over the 300 mV input range using an innovative resistive feedback DAC at the source terminal of the input differential pair.

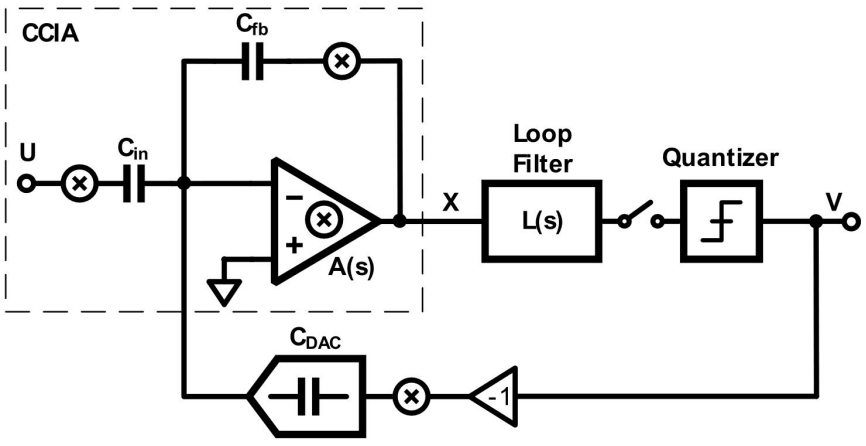

FIGURE 1.29 : Capacitively coupled instrumentation amplifier reducing the input driving requirements of the CT ΔΣ ADC. Reprinted from [154], © 2021 IEEE.

A final example can be found in [71], where an input impedance boosting technique is introduced for the DT loop filter. To minimize charge transfer in the switched-capacitor filter, the sampling capacitor is precharged with the previous output of the modulator just before the sampling phase. Since both voltage values are very similar, charge transfer is minimal, and the input impedance remains high. The input swing for this input stage is 600 mV_{pp} on a 1.3 V supply, and the input impedance reaches several MΩ, allowing for easy drivability.

1.8.5 SILICON AREA MINIMISATION DESIGN TRENDS

The active silicon area of an ADC design is of crucial importance due to its direct impact on cost. In semiconductor foundries, variable costs are mostly proportional to the number of silicon wafers produced. A larger die size will obviously result in a greater unit cost, which can have a very substantial incidence on viability at large-scale production. Hence, in order to maintain market competitiveness, it is essential to employ design techniques that minimize silicon area. This section focuses on the most area-efficient designs across various technology nodes. Because designs in newer technology nodes are inherently smaller than those in older nodes, comparisons are segregated across technology node sizes.

EFFICIENT USE OF HARDWARE

Many designs in the reviewed works leverage hardware sharing to maximize the utilization of on-chip resources. For instance, Zhang [37] introduces one of the smallest surveyed designs, featuring an NS-SAR with a hybrid EF-CIFF feedback path that reuses the same passive integrator for both paths. This design occupies a mere 0.012 mm^2 in a 28 nm technology node. Similarly, another NS-SAR design [100] incorporates a recycling integrator that reuses the same OTA to implement a 2nd-order loop filter, minimizing the area.

Other designs simply employ clever techniques to enhance hardware efficiency. Capacitors, particularly precise ones used in signal paths (e.g., metal-insulator-metal capacitors), tend to occupy significant chip area. To reduce the number of required capacitors, the DT ΔΣ design in [134] uses a buffer and a switching network to store the offset voltage of the integrator amplifier, eliminating the need for the usual auto-zero capacitor and significantly reducing area. Hwang [135] introduces a highly efficient inverter-based amplifier with a self-biasing scheme, reducing the entire amplifier design, including biasing, to just four transistors, along with a few switches and small capacitors. Finally, the novel CT NS-SAR design proposed in [103] and discussed in section 1.7.3 achieves the smallest surveyed design implemented in a 65 nm node, thanks to its efficient NS-SAR structure with a simple 1st-order loop filter.

HIGHLY DIGITAL ARCHITECTURES

Digital circuits are known for their ability to maintain a small area. Processing signals in the digital domain eliminates thermal noise constraints, thereby reducing the need for bulky capacitors. Transistors can also be smaller since no amplifier cells with stringent bandwidth and transconductance requirements are necessary. The topology that maximizes this principle is the TD ΔΣ modulator, which processes signals in the time domain. For instance, the TD ΔΣ discussed in [117, 121, 122] are among the top three smallest implementations in their respective technologies. Both [122] and [121] utilize a digital-like ring oscillator with a digital phase detector, while [117] employs a highly digital triangular CCO based on a switched capacitor bank.

Another example of a highly digital structure is the coarse stage of the zoom design by Jie [110]. This stage is implemented entirely digitally, utilizing an innovative counter structure

based on the digital output of the fine stage. This design is one of the smallest reported, occupying just 0.014 mm^2 in a 28 nm technology node.

NOISE MANAGEMENT TECHNIQUES

As previously mentioned, a common solution to reduce thermal noise is to make use of large sampling capacitors, which decrease the kT/C ratio. However, large capacitors necessarily occupy significant area. To alleviate this trade-off, kT/C mitigation techniques discussed in section 1.8.2 can be employed. Another approach used in two of the smallest NS-SAR implementations [29, 38] is to incorporate a dynamic amplifier before the passive filter in the NS-SAR feedback loop. This setup reduces the noise sampled on the filter by a factor proportional to the amplifier's gain, significantly decreasing the required capacitor sizes. In fact, [38] is the smallest of all the surveyed designs with an impressive active area of only 0.0049 mm^2 in a 28 nm node.

Another interesting technique used in Lee's design [46] with the second highest FOM_{Sc} is the use of pseudo-pseudo-differential amplifiers. These amplifiers are single-ended but coupled with switches to process signals differentially. One advantage of this approach is the simpler amplifier structure and the inherent flicker noise cancellation, allowing for significant area reduction. The DT $\Delta\Sigma$ design use three of these amplifiers for its 3rd-order loop filter, as illustrated in Fig. 1.30, yet it remains the smallest implementation in a 180 nm node, occupying only 0.0375 mm^2.

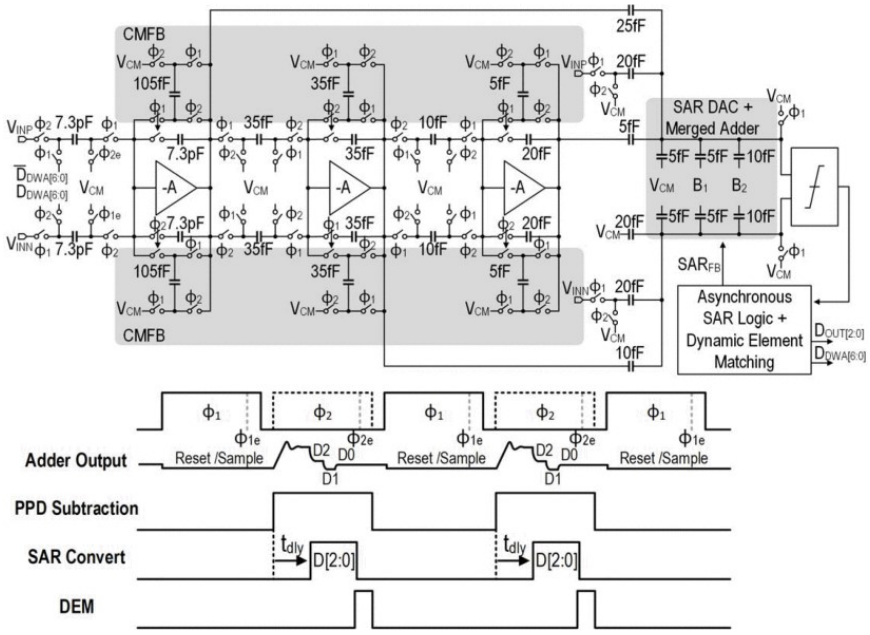

FIGURE 1.30 : Area- and power-efficient 3rd-order DT ΔΣ ADC leveraging pseudo-pseudo-differential amplifiers. Reprinted from [46], © 2022 IEEE.

1.8.6 PROCESS SCALING MITIGATION DESIGN TRENDS

Recent deep submicron technology nodes are highly power-efficient and allow for packing more features into a smaller area than ever before, at least as far as digital circuits are concerned. Despite the benefits in the digital domain, analog circuits such as ADC are instead presented with significant challenges. On one hand, the reduced supply voltage rail complexifies design due to decreased headroom, making it harder to maintain transistor stacks in the saturation region. On the other hand, reduced transistor length decreases output resistance, which limits gain and worsens matching. These issues are particularly critical in SoC design, where ADC are to be integrated with microprocessors for digital signal processing. The microprocessor is usually the main driver of the choice of a smaller technology node, which forces the ADC to be implemented in the same.

AMPLIFIER DESIGN

The primary component affected by technology scaling is the amplifier, where reduced supply voltage becomes a significant challenge. To address this, pseudo-differential amplifiers are often employed. These amplifiers eliminate the tail current source from the differential amplifier, thereby reducing the transistor stack. This approach is commonly seen in inverter-based amplifiers [107, 133, 134]. Inverter-based amplifiers are favored because they effectively double the available transconductance for the same bias current. However, a notable drawback of pseudo-differential amplifiers is the substantial reduction in power supply and common mode rejection ratio, as the branches of the amplifier no longer share the same current.

Similarly, pseudo-pseudo-differential amplifiers, which use the same single-ended amplifier for differential signal processing with alternate clocking, can be employed to reduce the transistor stack and simplify the circuitry [114]. The designs in [46, 54] also propose pseudo-pseudo-differential amplifiers, but they utilize a ring amplifier as the single-ended amplifier core. This approach makes the circuit even more scaling-friendly, as the ring amplifier presents a predominantly digital structure.

Simple loop filter structures, such as passive and buffer-based filters, limit the need for amplifiers and are also well-suited for digital-friendly, smaller technology nodes. These loop filter structures are covered in section 1.8.1, where detailed implementation information is provided.

THE TD $\Delta\Sigma$ TOPOLOGY

Another trend particularly well suited for tackling the challenges posed by smaller technology nodes is the TD $\Delta\Sigma$ architecture. Processing information in the time domain allows

for the use of digital-like circuitry, which scales effectively with advancing technologies. Additionally, the precision of time domain circuitry improves for smaller technology nodes due to reduced transition times. A prime example of such a design is presented in [125], where a VCO-based ΔΣ modulator is fully synthesized using hardware description language (HDL). The standard cell library is augmented with a few analog cells to facilitate the implementation of the mostly digital architecture. This design, implemented in 28 nm, can be more easily scaled to a smaller node than other designs by reusing the same HDL code and modifying the custom analog cells. Design examples that process information entirely in the time domain are covered in detail in section 1.7.5.

1.9 DISCUSSION

The design trends highlighted in this survey demonstrate the vast diversity and depth of possibilities in oversampling ADC design. A multitude of techniques are suited to achieve varied performance metrics, providing great flexibility in design choices. For instance, NS-SAR ADC excel at achieving outstanding power efficiency for moderate SNDR, while zoom ADC are unmatched for low bandwidth applications requiring very high precision. CT and DT ΔΣ ADC offer a more balanced package, enabling a wide range of performance trade-offs. In any topology, meticulous circuit-level design incorporating efficient loop filters, DAC linearization techniques, and thermal noise mitigation is crucial to achieve cutting-edge performance.

Navigating the diverse, intricate oversampling ADC architectures and implementations can be overwhelming. How does one select the most suitable ADC architecture and implementation parameters for their specific SoC requirements ? A method that is applicable on a heterogenous subset of oversampling ADC topologies is to simply compare designs based on a quantitative figure of merit such as FOM_{Sc}. Indeed, FOM_{Sc} captures the essential trade-off between bandwidth, power, and SNDR, which are clearly illustrated by the trendlines in

Figures 1.10 and 1.11. However, reducing the discussion to only three main performance characteristics may lead to a skewed assessment that overlooks critical elements for SoC implementation.

In research literature, oversampling ADC designs overwhelmingly exclude discussion of the crucial output decimation filter, which is typically implemented off-chip and thus not reflected in the disclosed ADC performance metrics. This omission is of particular significance because common foreground calibration methods used to improve DAC linearity (also often performed off-chip themselves) exacerbate the requirements of the decimation filter, due to an increased signal bit width to handle, all without adverse consequence in terms of FOM. On the contrary, on-chip MES techniques are unfairly penalized in published ADC performance metrics. Indeed, the additional power and area required by on-chip MES are included in the evaluation metrics, whereas the resulting streamlining of the off-chip decimation filter and calibration is not. Similarly, incremental $\Delta\Sigma$ ADC that utilize FIR-based decimation filters, which are simpler and consume less power, do not see these benefits reflected in the FOM when decimation is performed off-chip. In a practical scenario, all components of a SoC must obviously be present on-chip, including the decimation filter and the calibration circuits.

The input driving circuit of the ADC is another element often realized off-chip and thus overlooked in FOM calculations, but that is needed in a practical system. Indeed, most designs in literature do not explicitly include an input buffer amplifier, which would need to be as linear and low in noise as the ADC itself in order to meet requirements, resulting in stringent design constraints and requiring higher power rails than the ADC itself. For the rare designs that include an on-chip buffer, such as [177] and [179], its power consumption ends up being significantly higher than the rest of the entire ADC ! CT $\Delta\Sigma$ designs, due to their resistive input impedance and inherent anti-aliasing properties, can relax the input front-end requirements.

Certainly, conventional FOM are unable to account for these differences when the input buffer is located off-chip.

An interesting discussion on the topic was initiated by Nauta [6] in the latest ISSCC proceedings. Among other points, he explores the simple case of an amplifier driving a capacitive load representing a basic analog signal processing circuit, in an ADC for example, with a specified SNR requirement. In this scenario, it is shown that the minimal analog power consumption is :

$$P_{min} = \frac{V_{dd}}{V_s} \cdot 8 \cdot k \cdot T \cdot SNR \cdot f, \tag{1.14}$$

where V_{dd} is the supply voltage, V_s the input swing, k the Boltzmann constant, T the absolute temperature and f the signal frequency. It becomes apparent that a wider input swing V_s relative to supply voltage V_{dd} is beneficial for achieving lower ADC power consumption for a given SNR, thereby improving FOM_{Sc}. However, when the complex and power-hungry input buffer needed to handle a wider input swing is located off-chip, its own impact on total power consumption remains unaccounted for in FOM calculations. Therefore, Nauta proposes introducing a correction factor to FOM_{Sc} as follows :

$$FOM_{Sc+Bu} = FOM_{Sc} + 10\log\frac{V_{dd}}{V_s}. \tag{1.15}$$

This modified FOM credits designs for having a smaller input swing, as it should allow for relaxing the specifications of the input buffer, hence decreasing net aggregate system power consumption.

Another factor that remains completely left out by the habitual FOM is the cost effectiveness of the design under consideration. Even so, total implementation cost, which is a function of the semiconductor technology used and of the area footprint of the design, should be of the

utmost importance in practice. Indeed, designs implemented using recent technology nodes and occupying large silicon areas may involve a significantly high production cost, making them impractical for most mass-market applications.

To quantify cost effectiveness, it is reasonable to expect that it be proportional to the area of the active design. However, different technology nodes involve different cost scales, depending on their minimum feature size. For illustrative purposes, we propose a cost effectiveness factor (CEF) to be defined as

$$CEF = \frac{A}{tech^2}, \tag{1.16}$$

where A is the active design area (in μm^2) and $tech$ the technology node critical dimension (in μm). We apply this correction factor to FOM_{Sc} after having normalized it to the average of all designs in the study set to yield :

$$FOM_{Sc+Ar} = FOM_{Sc} - 10\log(CEF/\,\overline{CEF}). \tag{1.17}$$

This adjusted FOM penalizes designs presenting a less area-effective realization while rewarding designs that are likely to offer a cost advantage. It is worthy of mention that CEF as presented is neither intended as absolute nor definitive, but rather as a starting point on an indicative basis for taking into account design cost effectiveness. Indeed, the effects of technology scaling can often manifest in a varied and non-linear manner (e.g., different circuit component types may scale differently across technology nodes, distinct technologies may force the use of different techniques). Furthermore, CEF aims to assess the cost effectiveness of a *design*, not of a specific *implementation*. In other words, FOM_{Sc+Ar} would penalize a design requiring more area than a competitor implemented in the same technology. Ultimately, designers may be interested in such a metric to help them choose a suitable design topology, somewhat independently from the technology node selection. Certainly, any quality metric

can only ever be as good as the integrity of its constituent data. For instance, the placement off- or on-chip of auxiliary components such as input buffers, calibration circuitry or decimation filters may cause dramatic and artificial FOM_{Sc+Ar} variation, as the footprint of these parts gets inconsistently counted or not in the total design area. Nevertheless, through careful data validation, some interesting trends can be discovered.

It is also possible to combine the two aforementioned adjustments to generate $FOM_{Sc+Bu+Ar}$ so as to quantify ADC performance while also taking into account the impact of the input buffer as well as the cost effectiveness of the implementation.

These alternative FOM are presented in Fig 1.31, where the designs are ranked in descending order of FOM_{Sc}. For some designs, the four proposed FOM do not vary substantially. However, other designs significantly benefit from either their low input swing or their area efficient implementation. For instance, Lim's design [154], by virtue of an input swing of

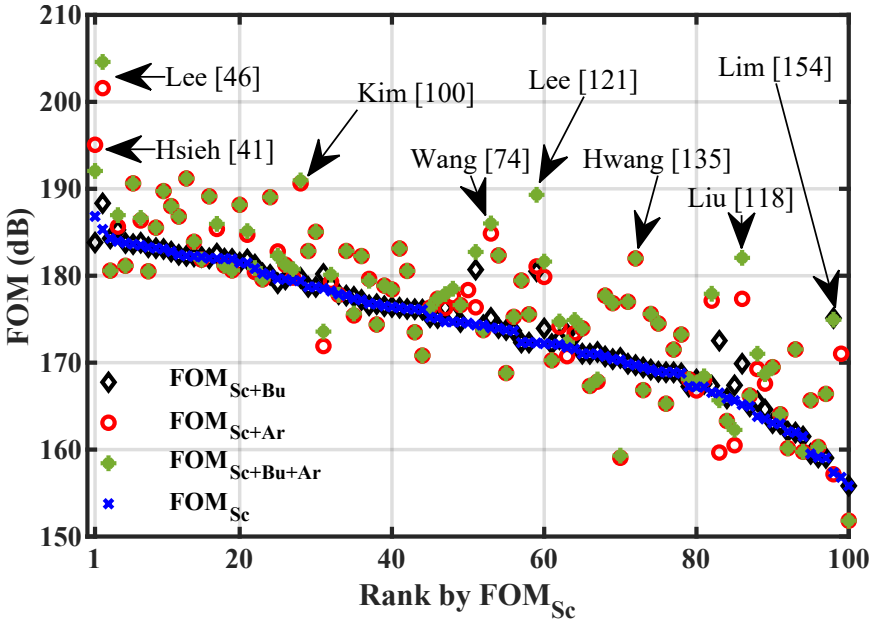

FIGURE 1.31 : Four alternate FOM with different correction factors applied, ordered by FOM_{Sc} rank.

only 60 mV, makes the input buffer design straightforward, which boosts its FOM_{Sc+Bu} by 17 dB. Kim's design [100] is very compact, occupying merely 0.12 mm^2 in a 180 nm node, which increases its FOM_{Sc+Ar} by 10 dB. Many designs benefit from their lower than average CEF, such as [74, 135], or from both criteria, such as [118, 121]. Interestingly, the top-FOM_{Sc} design by Hsieh [41], previously discussed in section 1.7.5, is penalized for its wide input swing of 2 V_{dd}, while the second-best FOM_{Sc} design by Lee [46] is highly area-efficient, surpassing Hsieh's design when using any of the three proposed corrected FOM. The fluctuation in top-ten ranking for the alternative FOM are highlighted in Table 1.1, showing that several

Rank	FOM_{Sc}	FOM_{Sc+Bu}	FOM_{Sc+Ar}	$FOM_{Sc+Bu+Ar}$
1	Hsieh[41]	Lee[46]	Lee[46]	Lee[46]
2	Lee[46]	Chand.[42]	Hsieh[41]	Hsieh[41]
3	Cheng[43]	Cheng[43]	Liu[106]	Liu[106]
4	Chand.[42]	Hsieh[41]	Kim[100]	Kim[100]
5	Lo[44]	Guo[49]	Karm.[50]	Karm.[50]
6	Karm.[50]	Lo[44]	Eland[48]	Eland[48]
7	Guo[49]	Karm.[50]	Wang[30]	Lee[121]
8	Mond.[45]	Mond.[45]	Liu[38]	Wang[30]
9	Liu[47]	Liu[47]	Gönen[107]	Liu[38]
10	Eland[48]	Eland[48]	Chae[32]	Gönen[107]

TABLEAU 1.1 : Best oversampling ADC designs ranked according to various FOM. Blue (red) shading intensity is related to higher (lower) FOM_{Sc} rank for this subset.

of the highest ranking ADC by FOM_{Sc} are overtaken by other designs when widening the breadth of the FOM to take into account some overlooked parameters.

Although these extra correction factors applied to Schreier's FOM can be very beneficial to designers trying to thin out and select an ADC architecture best suitable for specific needs, there exists no such thing as a perfect FOM. Some applications might find a design with a poor FOM to be the most suitable for their specifications due to idiosyncratic characteristics such as input impedance, decimation filter simplicity, ease of input multiplexing, low latency, superior anti-aliasing, etc. These are all important factors that fail to be simply encompassed in a single FOM equation. Though extremely challenging, this is precisely what sets ADC design apart as such a rich and interesting discipline. Indeed, there can exist as many design possibilities as there can be circuit specification combinations, making custom design often the most appropriate solution.

1.10 CONCLUSION

To conclude, the use of oversampling and noise shaping allows for unparalleled design flexibility at high precision, making the broad family of oversampling ADC the best suited to achieving high SNDR, as has been clearly depicted in Fig. 1.1 and 1.10. In the years to come, it appears likely that a promising trend would be innovation focusing holistically on full SoC implementation. With recent technology nodes, digital signal processing is becoming increasingly power-efficient, especially at high precision, since kT/C constraints do not apply in the digital domain. SoC-based ADC are poised to benefit from digitizing the signal as early as possible in the signal chain, with an input swing dictated by the application, thereby reducing the need for a resource-intensive input buffer amplifier. While research projects understandably often focus on specific issues like improving modulator efficiency, it would be

refreshing to see systemic innovations targeting the entire signal chain from input front-end to decimation filter.

Digital structures such as the TD $\Delta\Sigma$ topology will most likely play a predominant role in future designs as they scale better with technology and offer more headroom for power efficiency improvement. The main challenge to tackle will be to develop new techniques to linearize the time-domain processing circuit blocks. Dynamic circuits, such as FIA for loop filters, are a well-established trend that will surely continue to evolve, as many of the most power-efficient ADC ever designed incorporate this approach. Exciting and intriguing multi-loop structures combining different topologies are also expected to emerge, leveraging the strengths of multiple structures to achieve varied design trade-offs. One thing is clear : over-sampling ADC shall remain unavoidable in high-precision, high-performance data conversion for many years to come.

CHAPITRE II

A LEAN NOISE-CANCELLING STURDY MASH DELTA-SIGMA ADC WITH A NOISE-SHAPING SAR STAGE

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2.1 RÉSUMÉ EN FRANÇAIS

Ce papier introduit un ADC delta-sigma MASH à annulation de bruit réalisé grâce à l'implémentation d'un étage SAR à filtrage de bruit comme deuxième étage. L'usage de ce SAR au lieu de l'étage delta-sigma conventionnel élimine, de par son mécanisme de feedforward inhérent, le bruit de quantification du premier étage. De plus, les erreurs induites par le mismatch dans le SAR à filtrage de bruit sont filtrées par le premier étage, contournant le besoin d'avoir de strictes contraintes de matching dans les condensateurs ou une calibration additionnelle. L'élimination des circuits d'annulation de bruit et de calibration de même que l'utilisation du SAR à filtrage de bruit efficace rendent cette topologie très peu encombrante. Les simulations démontrent une preuve de concept atteignant 107.7 dB de SQNR pour un OSR de 14 sur une bande passante de 1 MHz.

2.2 ABSTRACT

This paper introduces a lean noise-cancelling sturdy-MASH delta-sigma ADC, achieved through the implementation of a noise-shaping SAR second stage, the use of which instead of the usual delta-sigma stage, eliminates, by virtue of its inherent feedforward mechanism, the quantization noise of the first stage. Moreover, any mismatch-induced error of the noise-shaping SAR gets shaped by the first stage, circumventing the need for strict capacitor matching or calibration. The elimination of noise-cancelling and/or calibration circuitry, as well as the inclusion of the area-efficient noise-shaping SAR qualify this topology as lean. Simulations demonstrate a proof-of-concept design achieving 107.7 dB SQNR for an OSR of 14 over a 1 MHz bandwidth.

2.3 INTRODUCTION

In this budding era of widespread implementation of Internet of Things (IoT) and wireless sensor networks (WSN), the demand for high precision, low-power analog-to-digital converters (ADC) has never been greater. Such applications prioritize high signal-to-noise ratio (SNR), power efficiency and cost effectiveness, while a relatively low bandwidth of up to 1 MHz is typically sufficient to meet the requirements [94].

Noise-shaping successive approximation (NS-SAR)[27] is a promising architecture to meet the needs of sensor networks. Incorporating a SAR quantizer within an error-feedback delta-sigma ($\Delta\Sigma$) topology, the NS-SAR architecture is power-efficient, low cost and process scaling friendly[28]. However, to achieve high SNR, the signal-dependent error of the SAR's capacitive digital-to-analog converter (CDAC) must be limited, typically by means of foreground calibration[28, 94], increasing complexity and power consumption.

The ΔΣ architecture has long been a candidate for high SNR applications, but it is vulnerable to process scaling as it struggles with the reduced transistor gains of recent technology nodes[180]. Another inconvenience of ΔΣ ADC is the limited practical bandwidth due to high oversampling ratio (OSR). OSR can be reduced for higher order modulator noise-shaping, at the price of stability problems[7].

To overcome the respective limitations of the NS-SAR and ΔΣ architectures, combinations of both structures have been proposed. Multi-stage noise-shaping (MASH)[51] structures combine two stages of ΔΣ modulators to increase noise-shaping order, cancel the first stage error and alleviate stability problems[7]. However, tight matching between the analog and digital circuit blocks is required to combine the two stages, which poses a challenge as PVT variations can introduce mismatch and degrade SNR due to noise leakage[7]. Several combinations of NS-SAR in MASH structures have been proposed, for example two NS-SAR in a conventional MASH[181] or a pipeline MASH structure[58].

To alleviate the mismatch sensitivity inherent to the MASH architecture, the sturdy MASH (SMASH) architecture was introduced, which relies on analog feedback rather than digital cancellation to combine the two stages, eliminating the need for precisely matched digital blocks[64]. However, in SMASH, the error of the first stage is no longer cancelled, but merely attenuated by the high order noise-shaping[7]. Noise-cancelling SMASH (NC-SMASH) has been proposed to eliminate the error of the first stage like in MASH, but delay matching or additional circuit blocks are then necessary[65, 68]. Either SMASH or NC-SMASH incorporating a NS-SAR stage has yet to be explored.

This work proposes a discrete-time (DT) lean NC-SMASH (LNC-SMASH) ΔΣ ADC with a NS-SAR second stage. In this novel topology, the noise of the first stage is cancelled by a fast path provided by the inherent feedforward property of the NS-SAR second stage[28].

Since the first stage error is nullified, a quantizer with a low bit count can be used to minimize power consumption and size for that DT ΔΣ stage. As for the remaining error originating within the NS-SAR second stage, it is shaped by the filters in both the first and second stages, ensuring a high SNR at low power consumption. In addition to these benefits, the proposed architecture improves overall robustness and relaxes design constraints by having signal-dependent errors of the second stage shaped by the DT ΔΣ first stage. As a result, the potential of the proposed ADC is very promising for high precision, low-power applications.

This paper begins with a brief review of SMASH and a description of the proposed architecture in section 2.4. Simulation results are discussed in section 2.5, while section 2.6 presents the conclusions of this work.

2.4 SYSTEM OVERVIEW

2.4.1 LIMITATIONS OF THE SMASH ARCHITECTURE

Fig. 2.1 shows the block diagram of a classic SMASH ΔΣ ADC. Unlike the MASH structure, this configuration eliminates the need for separate digital filters because signal combination occurs before filtering. This relaxes the op-amp gain requirements necessary to obtain proper matching between analog and digital sections[64]. The transfer function of the SMASH structure is :

$$D_{out}(z) = STF_1 V_{in}(z) - NTF_1 NTF_2 E_2(z) + NTF_1(1 - STF_2)E_1(z), \tag{2.1}$$

with STF_n and NTF_n respectively the signal and noise transfer function of the n^{th} stage. Generally, STF_2 is designed to be equal to $1 - NTF_2$ so that the error of both stages is shaped by the same transfer function[7]. In that case, to achieve a given SNR, both stages must have the same bit count, tightening design constraints and increasing area.

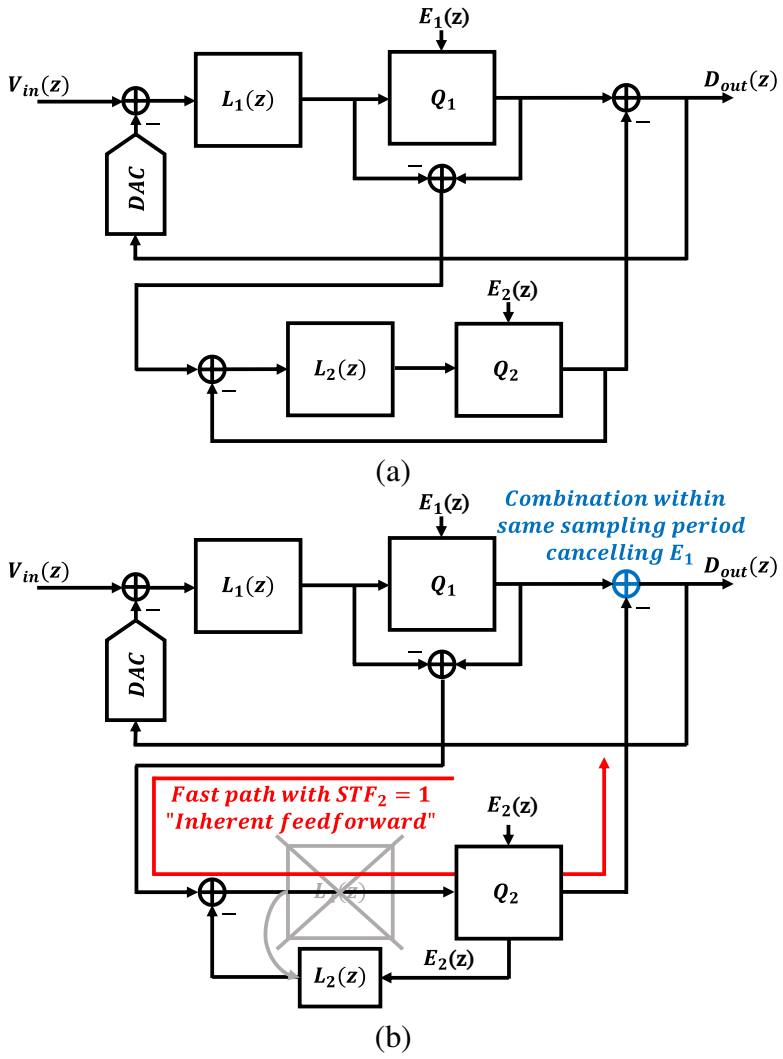

FIGURE 2.1 : Diagram of (a) the SMASH architecture and (b) the novel LNC-SMASH architecture. Reprinted from [9], © 2023 IEEE.

The appealing option of instead setting $STF_2 = 1$ to completely cancel the noise of the first stage would require a delay-free transfer function for the second stage, which is only archivable with an additionnal feedforward path and tighter timing constraints, increasing power consumption and area [7, 64]. The NC-SMASH in[68] introduces a delay, as well as a compensation DAC, to maintain stability, so that the term $(1 - STF_2)$ in (2.1) transforms into

$(z^{-1} - STF_2)$, resulting in an easier to implement signal transfer function of z^{-1} to cancel E_1, albeit at the expense of added circuitry.

2.4.2 SYSTEM-LEVEL IMPLEMENTATION

The modifications proposed in the new LNC-SMASH architecture are presented in Fig. 2.1. By using a NS-SAR in the second stage, a fast path is created between input and output of the second stage by virtue of the relocation of the loop filter onto the error feedback path. Achieving STF_2 of 1 without added delay is now straightforward as there are no longer any integrators on the signal path. Provided that the quantizer is sufficiently fast to deliver its output within the same sampling period, combination will be able to occur before the next sample is captured. In[28], the NS-SAR topology is deemed "inherently feedforward" due to the signal path avoiding the loop filter. From (2.1), the unity STF_2 of the NS-SAR allows for cancellation of the quantization noise of the first stage, such that :

$$D_{out}(z) = STF_1 V_{in}(z) - NTF_1 NTF_2 E_2(z). \tag{2.2}$$

This effect has the important benefit of relaxing the constraints on the bit count of the first stage quantizer, which results in a more favorable trade-off between power, area, and SNR.

Fig. 2.2 presents a detailed block diagram of the proposed system-level implementation. The first stage consists of a DT $\Delta\Sigma$ structured as a cascade of integrators with feed forward (CIFF). DT implementation is selected for its robustness since loop coefficients depend on capacitor ratios instead of RC time constants[7]. CIFF is chosen for its low power and low distortion due to reduced amplitude swing in the integrators and only one DAC needed for feedback. The use of a SAR quantizer in this stage is optimal because it is able to directly

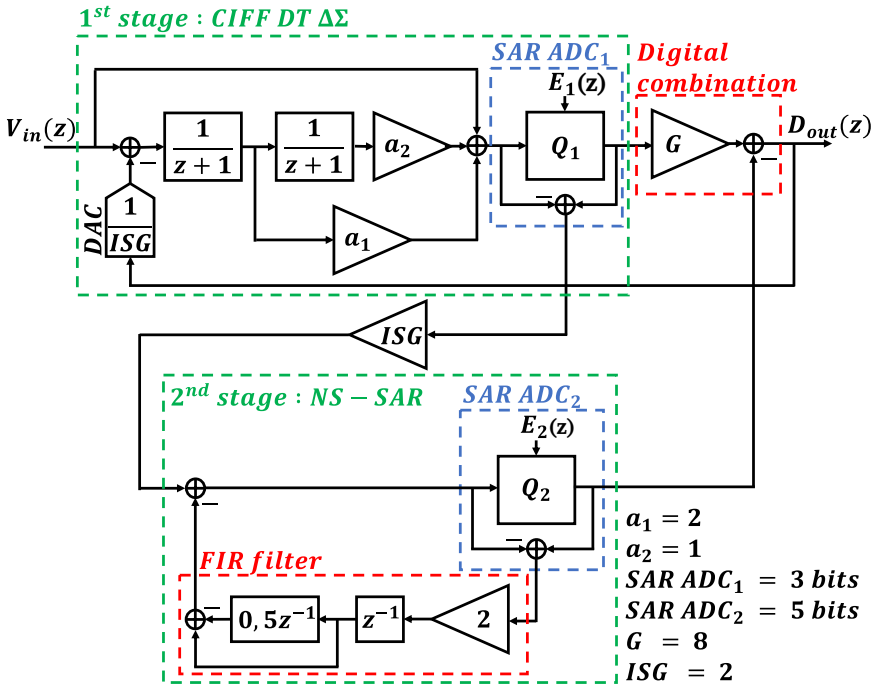

FIGURE 2.2 : Diagram of the proposed LNC-SMASH with NS-SAR stage. Reprinted from [9], © 2023 IEEE.

generate the residue error for the second stage, eliminating the need for any additional adder or DAC component.

As for the second stage, NS-SAR is sensitive to non-linear errors on its SAR CDAC and FIR filter. These error sources introduce harmonic distortion in the signal and can be modeled as additive noise sources [28]. By having a DT ΔΣ as the first stage, these errors will be shaped by NTF_1, mitigating their impact. As such, the matching and linearity requirements of the NS-SAR are relaxed so that calibration is no longer essential, further lowering the power and area needs of the already-efficient NS-SAR stage.

The combination of the two stages is performed by means of a digital adder so that the subtraction is error free and to remove the need for an additional feedback DAC. A gain G of 8 is added in series with the output of the first stage to bring the 3-bit $SAR\ ADC_1$ to the

same scale as the 5-bit *SAR* ADC_2. An interstage gain (ISG) of 2 is also included to make use of the entire second stage quantizer range and improve signal-to-quantization-noise ratio (SQNR)[182]. The subsequent division by 2 is implemented in the feedback DAC, which contains 96 unit elements with halved weight.

The proposed topology is qualified as "lean" because it allows important reduction of the requisite circuit blocks in comparison to a standard NC-SMASH. The inherent feedforward of the NS-SAR stage provides noise cancelling without the cost of added circuitry, while relaxing the constraints on the first stage. Furthermore, the NS-SAR stage itself is highly area efficient as it doesn't require calibration and the loop filter is simpler than in the $\Delta\Sigma$ counterpart. Finally, the use of SAR quantizers in each stage allows the provision of the error signals without the need for additional DAC and summers.

The noise cancellation decreases the input levels processed by the quantizers and the loop filters, reducing the risk of saturation and making aggressive NTF achievable with a looser constraint on maximum input amplitude. All gain coefficients in the system are designed to yield $(1-z^{-1})^2$ for both NTF.

2.4.3 PROOF-OF-CONCEPT DESIGN

A proof-of-concept design intended for a 65 nm node with 1.2 V supply was realized at system level to test the new architecture. The design aims for a target signal-to-noise-and-distortion ratio (SNDR) superior to 90 dB after fabrication, with a 15 dB margin. To determine the requisite OSR and quantizer number of bits, the following theoretical SQNR expression is used[7, 182] :

$$SQNR_{dB} = 10\log\frac{6A^2(2L+1)OSR^{2L+1}ISG^2}{\pi^{2L}\Delta^2}, \tag{2.3}$$

with A the input amplitude, L the modulator noise-shaping order and Δ the voltage interval between 2 quantizer levels in the second stage. It is determined that a 5-bit quantizer with an OSR of 14 yields a theoretical SQNR of 107.8 dB for an input of -3 dBFS, meeting design requirements. Expected bandwidth is 1 MHz for a 28 MS/s sampling rate.

2.5 SIMULATION RESULTS

System-level simulations were conducted in MATLAB and Simulink as a first proof of concept for the new ADC architecture. Parts of the model and functions used for calculation were inspired by Schreier's toolbox[7, 183].

2.5.1 SIMULATION OF IDEAL OUTPUT SQNR

Fig. 2.3 presents the output power spectrum density (PSD) for -3 dBFS input at 100 kHz. It can be observed that the noise shaping slope is indeed -80 dB/dec confirming the 4^{th} order modulator behaviour. Simulated SQNR is 107.7 dB which is very close to the theoretical calculation of 107.8 dB with (2.3).

Fig. 2.4 compares the output SQNR at varying OSR for the proposed LNC-SMASH compared to simulated scenarios based on 1) the 2-2 SMASH of [64] with a 3- and a 5-bit quantizers (same as this work), 2) that 2-2 SMASH again but with two 5-bit quantizers (to account for its first stage not benefiting from noise cancellation) and 3) the second-order NS-SAR of [184] with a 7-bit quantizer (overall capacitor footprint similar to this work). The proposed LNC-SMASH topology achieves the best noise-shaping throughout the evaluated OSR due to its noise cancellation, high order noise shaping and efficient synergy of the two stages.

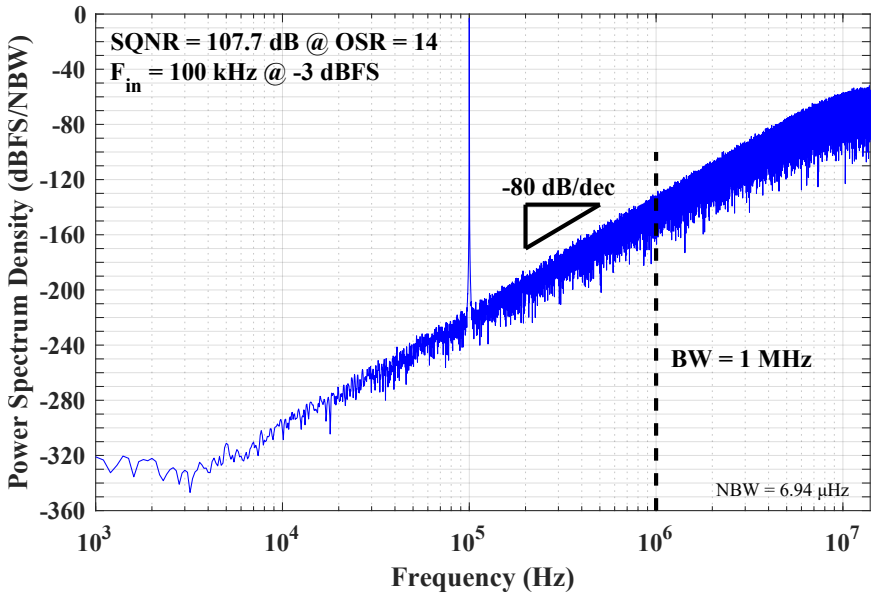

FIGURE 2.3 : Simulated output power spectrum density of the proposed ADC. Reprinted from [9], © 2023 IEEE.

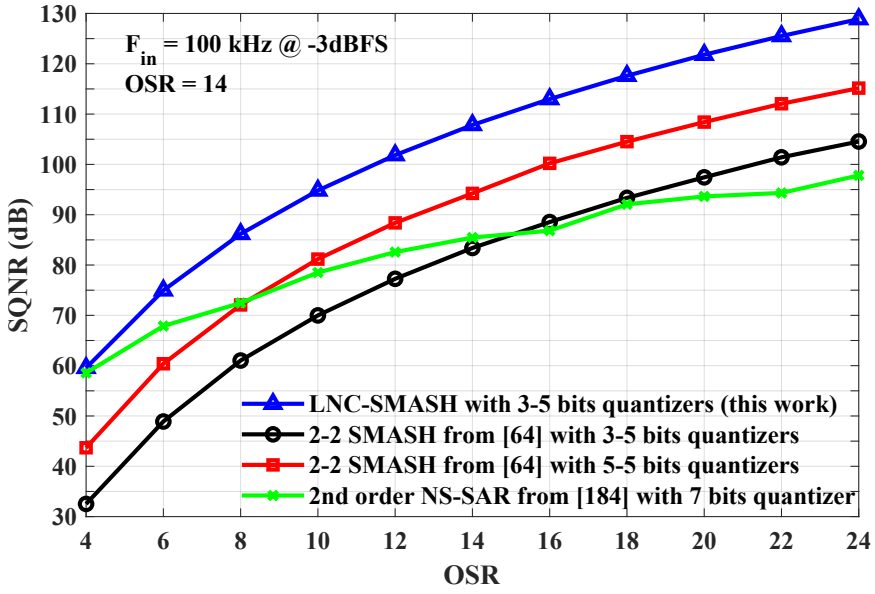

FIGURE 2.4 : Comparison of the SQNR for the LNC-SMASH of this work with a 2-2 SMASH and an NS-SAR with equivalent capacitor area. Reprinted from [9], © 2023 IEEE.

Fig. 2.5 shows the effect of varying input amplitude on SQNR. Peak SQNR of 110.3 dB is achieved for -0.75 dBFS. The dynamic range (DR) is 110.8 dB.

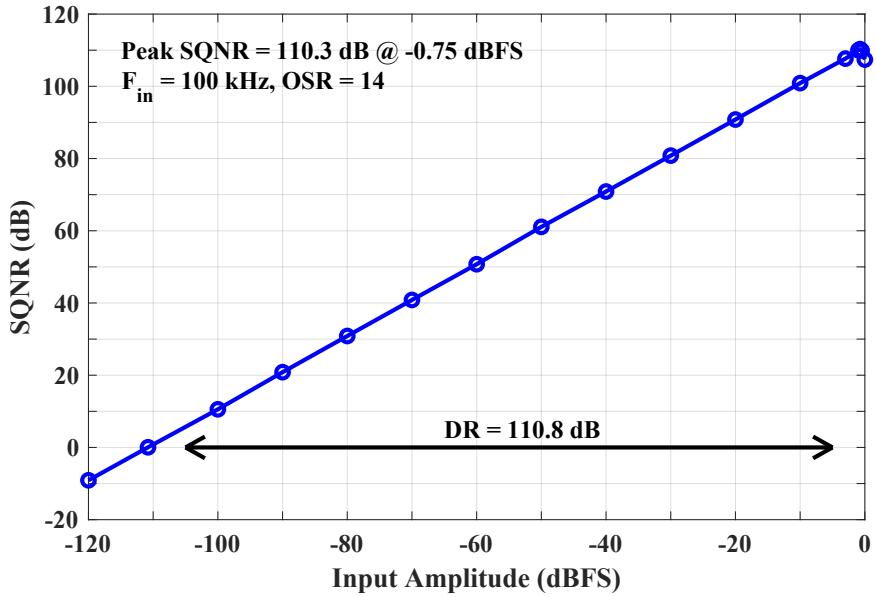

FIGURE 2.5 : Simulated SQNR with varying input amplitude. Reprinted from [9], © 2023 IEEE.

2.5.2 SIMULATION OF MISMATCH EFFECT ON SNDR

Assuming CDAC-based SAR quantizer and capacitive feedback DAC outputting in the switched capacitor integrator of the first stage DT ΔΣ, the main sources of non-linearity in the proposed ADC arise from any capacitor mismatch in these circuit blocks. To study these non-ideal behaviors, as presented in Fig. 2.6, a first Monte Carlo simulation (50 iterations, 10kHz -3dBFS sine input) was realized to compare sensitivity to capacitor mismatch in the NS-SAR stage's CDAC for the proposed architecture, as well as for the isolated NS-SAR. In a classical NS-SAR, CDAC errors do not get shaped and severely degrade SNDR. On the other hand, with the proposed SMASH architecture, NS-SAR's CDAC errors get shaped by the DT ΔΣ first stage and become less of a concern, removing the need for calibration.

A similar study was performed to compare the impact of capacitor mismatch within both stages' SAR quantizers and main feedback DAC, as presented in Fig. 2.7. Contrary to the errors of the SAR quantizers, the error of the main feedback DAC does not get shaped. As

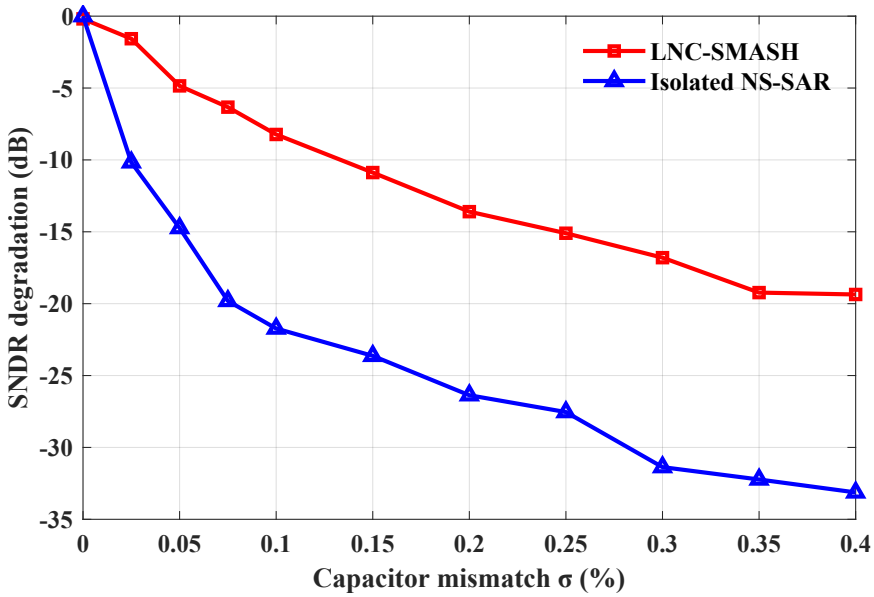

FIGURE 2.6 : Monte Carlo simulation of the SNDR degradation from the capacitor mismatch in the NS-SAR stage's CDAC for the proposed LNC-SMASH vs the isolated NS-SAR second stage with 10kHz -3dBFS sine input. Reprinted from [9], © 2023 IEEE.

such, the rapid deterioration of ideal SQNR relative to capacitor mismatch is striking, whereas SAR CDAC mismatch is not of concern, even when aiming for SNDR above 90 dB.

A simple first order element rotation "data weight averaging" (DWA)[169] was also tested in simulations to mitigate the deleterious effects of main DAC mismatch. Despite improved robustness, the SNDR still falls short of the 90 dB target. As such, calibration or higher order mismatch shaping would be necessary to achieve the desired SNDR. Nevertheless, the proposed architecture achieves a significant relaxation of the matching constraints of both SAR quantizers and NS-SAR FIR filter. High linearity requirements are now concentrated in one block : the main feedback DAC, which is a common issue for every ΔΣ ADC. Further research should be pursued to elaborate new solutions to improve this critical block.

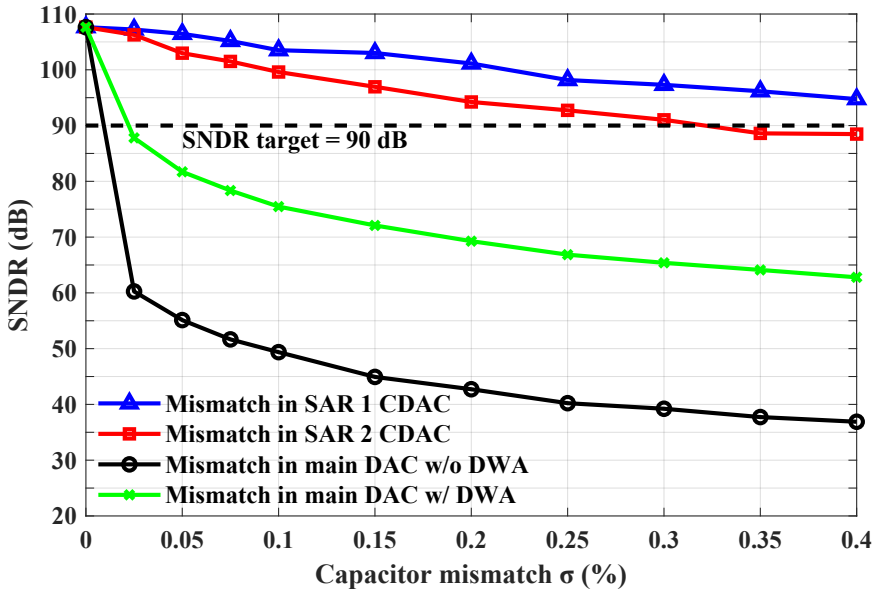

FIGURE 2.7 : Monte Carlo simulation of the SNDR of the proposed LNC-SMASH for different capacitor mismatch sources with 10kHz -3dBFS sine input. Reprinted from [9], © 2023 IEEE.

2.6 CONCLUSION

In conclusion, this paper introduced the LNC-SMASH ADC architecture featuring a NS-SAR stage for the first time. The inclusion of NS-SAR allows for the cancelling of the first stage's quantization noise, similarly to the MASH structure. Furthermore, the DT $\Delta\Sigma$ implementation of the first stage shapes the signal-dependent error of the NS-SAR second stage, relaxing the matching and linearity constraints. System-level simulations demonstrate a functional proof of concept and promising results for high precision, low-power applications.

CHAPITRE III

A RAIL-TO-RAIL LOW-POWER DYNAMIC CMOS AMPLIFIER FOR SWITCHED-CAPACITOR FILTERS IN HIGH-PERFORMANCE ADC

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3.1 RÉSUMÉ EN FRANÇAIS

Ce papier présente un nouvel amplificateur dynamique CMOS rail-à-rail basse puissance optimisé pour les filtres à temps discret dans les convertisseurs analogiques-numériques. L'architecture proposée exploite une technique de compensation parallèle résistive-capacitive commutée qui est stratégiquement activée durant la phase d'échantillonnage pour minimiser la consommation de courant de l'amplificateur. La polarisation dynamique de l'amplificateur améliore encore davantage l'efficacité énergétique en réduisant les courants de slewing une fois la phase de convergence linéaire atteinte. Des simulations en CMOS 65 nm montrent une réduction par 3.2 fois de la consommation de puissance par rapport à un amplificateur statique équivalent. Des formes d'ondes précises sont atteintes en consommant à peine 239 μW pour une stabilisation 6 τ en 4.9 ns.

3.2 ABSTRACT

This paper presents a novel rail-to-rail low power dynamic CMOS amplifier optimized for discrete-time filtering in analog-to-digital converters (ADC). The proposed architecture incorporates a switched resistor-capacitor (RC) parallel compensation technique, which is strategically activated in the sampling phase to minimize the amplifier's current consumption. Dynamic biasing of the amplifier further improves energy efficiency by slashing high slewing currents once linear settling takes over. Simulation results in 65 nm CMOS exhibit 3.2 times reduction in power consumption with respect to a comparable static amplifier. Accurate integration waveforms are achieved while consuming a mere 239 μW for 6 τ settling under 4.9 ns.

3.3 INTRODUCTION

With the ever shrinking transistor sizes in deep submicron technology nodes, analog designs are more challenging than ever. Indeed, the reduced supply voltages impose significant circuit constraints as the exploitable headroom is compressed. To make things worse, system specifications are also increasingly demanding. In portable, battery powered, embedded applications like sensor nodes or edge AI, every microjoule of energy must be squeezed to optimize autonomy and battery size. At the same time, such systems integrate complex analog building blocks, mainly high-performance analog-to-digital converters (ADC) to interface with sensors. These blocks typically require amplifiers to process analog signals, which tend to be among the most power-hungry circuits[185].

To meet these ever-tightening design constraints, state-of-the-art data converters propose many ingenious strategies for lowering power consumption while improving performance. One interesting solution dating back to the late 70s is the dynamic amplifier[139, 140]. Contrary

to a standard amplifier with static biasing, the biasing current of a dynamic amplifier is not constant, but rather varies during the amplification phase. Dynamic amplifiers are intended for discrete-time signal processing applications as their output varies with time and requires a periodic cycle to be processed, which is a perfect match for discrete-time ADC based on switched capacitors (SC). The ability to vary the biasing current of the amplifier during its operating cycle allows for better balancing of power usage.

Dynamic amplifiers come in a plethora of topologies. Some make the bias current input dependent[141], while others refine the more classical design of a discharging capacitor inside a differential pair gain stage[142, 143]. Polyphase amplifiers switch resistors during operation to adjust amplifier properties[94, 186]. Other innovative dynamic amplifier topologies have been proposed such as the floating inverter amplifier, first presented as a StrongARM latch preamplifier[187], and then in noise-shaping SAR as the loop filter[101].

The driving principle of these topologies is to make the amplifier properties vary with time in order to reach a better tradeoff between power consumption, amplifier response, settling time and noise. However, they usually rely on discharging a capacitor, which reduces output swing and limits settling speed.

This work proposes a different approach to the dynamic amplifier based on a 2-stages amplifier with a rail-to-rail, class AB output stage with high drive capability. The design is intended to serve as the amplifier inside a switched-capacitor integrator, meant to be used as loop filter in a discrete-time $\Delta\Sigma$ ADC. The operation of the dynamic amplifier takes place in two parts. Firstly, the compensation of the amplifier is dynamically adjusted to always satisfy phase margin while simultaneously keeping capacitive loading at a minimum. Secondly, the bias current of the input stage is dynamically controlled with a switched-ratio dynamic current mirror, allowing the biasing current to be reduced as the amplifying phase progresses. This

approach allows ample current for fast slewing, while preserving low power consumption when linear settling occurs further down the settling phase.

This paper is organized in three sections. First, section 3.4 covers the proposed rail-to-rail dynamic amplifier topology. Next, section 3.5 presents a SC integrator design within a ΔΣ ADC with simulation results. Finally, a conclusion wraps up the article.

3.4 PROPOSED AMPLIFIER TOPOLOGY

3.4.1 DESIGN OVERVIEW

The target application of the dynamic amplifier is as a fully differential amplifier inside a SC integrator circuit (inspired from[7]) as shown in Fig. 3.1. This circuit is a typical loop filter in discrete-time ΔΣ ADC and is the proposed use case of the novel dynamic amplifier topology. The amplifier is specifically tailored to be working in this topology for reasons that will become evident soon.

The proposed dynamic rail-to-rail amplifier is presented in Fig. 3.2. The main idea is to form a differential pair as the first stage, coupled with a rail-to-rail Class AB second stage,

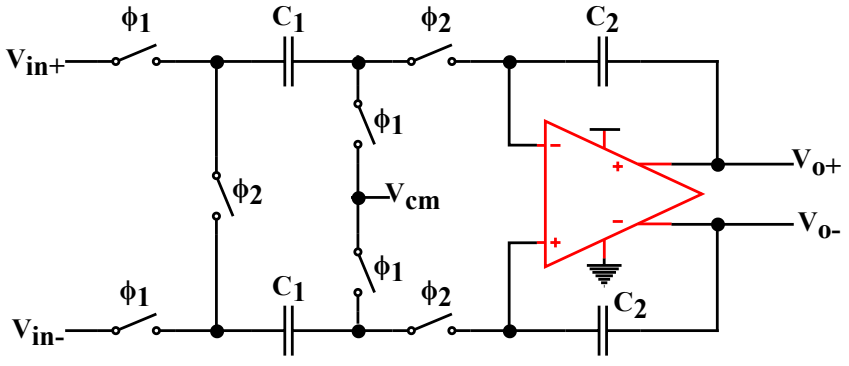

FIGURE 3.1 : Schematic of the switched-capacitor integrator targeted by the amplifier design. Reprinted from [10], © 2024 IEEE.

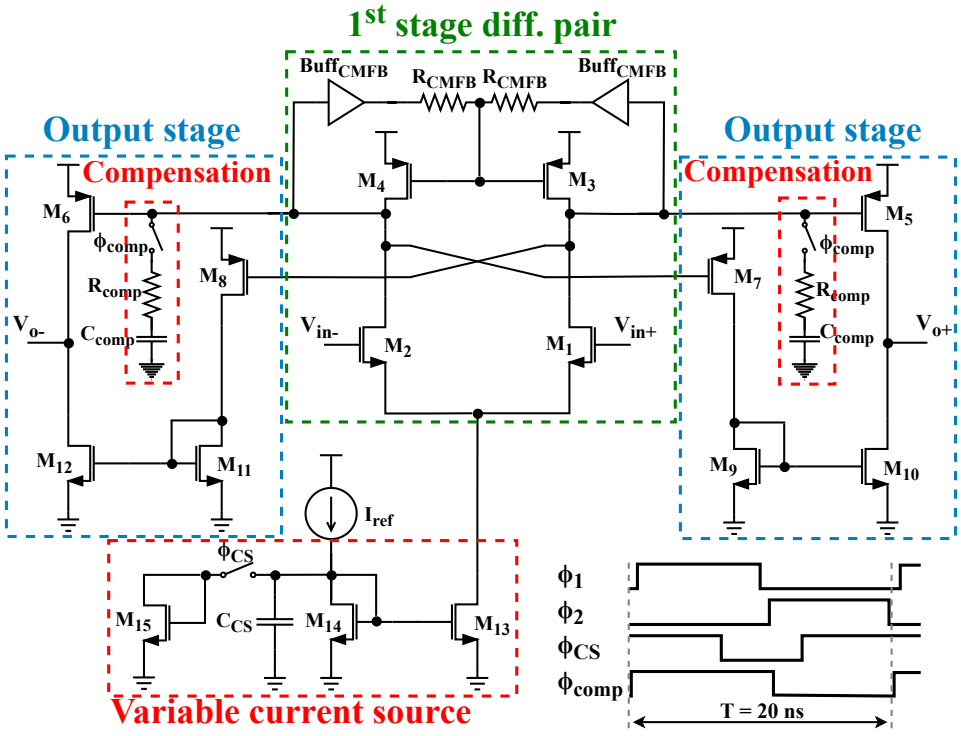

FIGURE 3.2 : Schematic and clock diagram of the proposed low-power rail-to-rail dynamic amplifier. The common-mode feedback of the output stage is omitted for clarity. Reprinted from [10], © 2024 IEEE.

featuring time-varying biasing and stability compensation. The amplifier compensation can be turned off during the main amplification phase of the SC circuit (ϕ_2 in Fig. 3.1) so as to greatly reduce capacitive loading and hence current requirements of the first stage. Varying the bias current of the same differential pair allows for further reduction of power consumption by yielding a more efficient bias point after the slewing phase during settling. Moreover, the resistive common-mode feedback (CMFB) shifts the bias point of the output stage as the current varies, allowing optimization of the power consumption of both stages only by controlling one current source. High amplification gain is achieved through the cascade of the two stages. Each part of the circuit is explained in more detail below.

3.4.2 FIRST STAGE

The first stage is a fully differential pair with active load. The input NMOS ($M_{1,2}$) are biased in subthreshold to achieve high transconductance, hence high gain, efficiently. The active load PMOS ($M_{3,4}$) are in moderate inversion so that their transconductance is just below that of $M_{1,2}$ to reduce thermal noise, as will be explained in a following subsection.

The biasing of the first stage is ensured by a variable current source. The core concept behind varying the bias current of the amplifier is its operation in a discrete-time, settling-based context, where the input arrives in steps from the previous discrete sample. Convergence toward the settling point occurs in two phases : a slewing phase, followed by a linear settling phase. Both phases require different bias currents, slewing being generally the most power hungry. One can ensure fast slewing by providing sufficient biasing current during that phase, while decreasing biasing current as much as possible during the linear settling phase to save on power.

The CMFB of this first stage consists of two buffers with two resistors, enabling fast common-mode extraction without loading the stage nor reducing its gain. Fast CMFB is necessary to accurately track the common-mode changes as the bias current varies during amplification. This common-mode scheme allows the adjustment of the common mode in response to current variations. Specifically, reducing the bias current in the differential pair during amplification decreases the overdrive voltage of the active load PMOS ($M_{3,4}$), consequently increasing the output common-mode DC voltage through the CMFB. The rising common mode at the output of the first stage changes the biasing of the second stage, enabling it to achieve the same power savings as the first stage.

The optimal biasing current was determined considering high-level simulation settling performance and design complexity. To maintain the design as simple as possible while ensu-

ring good performance, an exponential current waveform was selected. Although switching the current in a stepwise manner is easier to implement (saving capacitor C_{CS}), sharp current transitions may cause undesirable swings in the DC operating point of the amplifier. The waveform of the biasing current and the output common mode of the first stage are presented in Fig. 3.3 to better illustrate the concept.

3.4.3 VARIABLE CURRENT SOURCE

The variable current source consists of $M_{13\text{-}15}$, switch ϕ_{CS}, capacitor C_{CS} and a copy of the reference current source of the IC, represented by the DC source I_{ref} in Fig. 3.2. The objective is to reliably generate an exponentially descending current between two DC values. A process-voltage-temperature (PVT) robust method for achieving a step change in

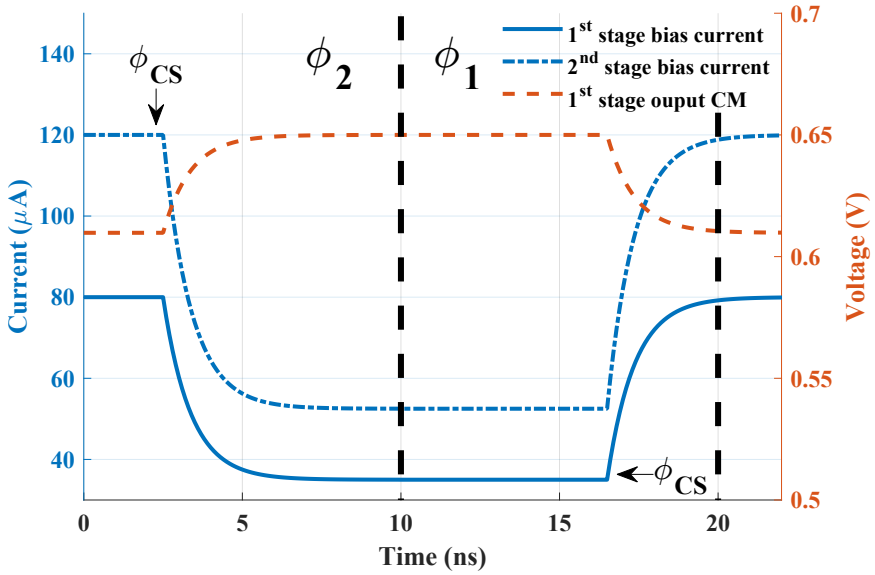

FIGURE 3.3 : Ideal waveform of the biasing current during amplification (ϕ_2) and sampling (ϕ_1) phases, highlighting the change in common mode voltage between the two stages caused by current variation in the first stage. Reprinted from [10], © 2024 IEEE.

current involves the use of a current mirror with a varying ratio. The current is determined by I_{ref} times the size ratio M_{13}/M_{14} for the high current at the beginning of the amplifying phase when ϕ_{CS} is open. Afterwards, as ϕ_{CS} closes, the current shifts towards I_{ref} times the size ratio $M_{13}/(M_{14}+M_{15})$, shifting the current to a lower value. The transition between the initial and final current values is smoothed by capacitor C_{CS} to emulate an exponential curve. Mathematically deriving the waveform for ideal MOSFET and switches results in a hyperbolic tangent current waveform, which can be closely approximated to the desired exponential curve in Fig. 3.3 through precise device sizing.

3.4.4 OUTPUT STAGE

The output stage is a class AB output stage inspired from[21]. It consists of PMOS $M_{5,6}$ in a common-source amplifying stage, with a current mirror drawing input from the opposite polarity branch as its source of biasing. Through this arrangement, the biasing current of the stage is increased in the event of a large swing input : as one of the differential output nodes of the first stage is pulled down, the bias current through the mirror rises, thereby enhancing drive capability and limiting slewing.

The varying common mode at the input of $M_{5,6}$, which follows the variable bias current of the first stage, also allows for the biasing of this stage to be varied by adjusting the level of the biasing output mirrors, as illustrated in Fig. 3.3. Consequently, both stages can benefit from higher current for slewing at the beginning of the amplification phase, and lower current during linearly settling towards the end of the phase.

The CMFB of this stage (not depicted in Fig. 3.2), is achieved through resistive sensing, followed by an error amplifier with a reference voltage fixed at the desired common mode. This amplifier then acts on the gates of two additional NMOS transistors in parallel with M_{10}

and M_{12} to adjust the current necessary to maintain an accurate common mode at half the supply voltage, ensuring rail-to-rail swing.

3.4.5 STABILITY AND SWITCHING COMPENSATION

To minimize power consumption, the dominant pole is strategically placed at the output of the amplifier, where large switched capacitors are located due to the integrator topology in which the amplifier is inserted, avoiding the need for an additional dominant Miller compensation. Furthermore, simulations have demonstrated that the combination of large switched capacitors and switch resistance introduces a zero in the frequency domain, providing adequate phase margin to ensure stability during the amplification phase as shown in Fig. 3.4. However, once the amplification phase ends and switches are closed, this zero vanishes as the switched-off resistance becomes too large, and the phase margin drops to a dangerously

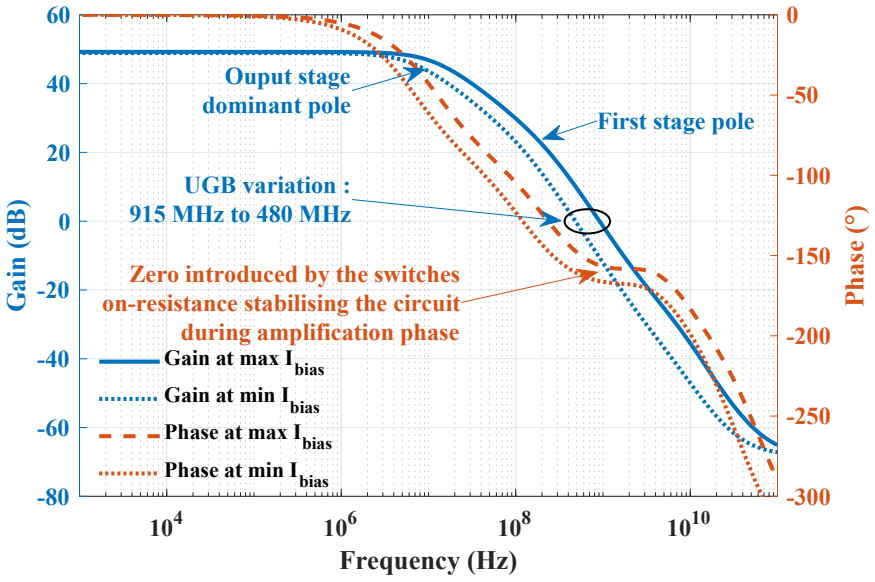

FIGURE 3.4 : Simulation results of the AC response of the proposed amplifier during the amplification phase for the highest and the lowest varying bias current. Reprinted from [10], © 2024 IEEE.

low level. Consequently, a RC compensation network is activated with ϕ_{comp} during the sampling phase and deactivated as soon as the amplification phase begins. This approach allows the amplifier to maintain a sufficient phase margin throughout its operation while avoiding capacitive loading during the amplification phase. As such, this approach reduces the current requirement for the first stage differential pair. Transient waveform disruption caused by the additional circuit switching is minimal and occurs at the beginning of the phase, ensuring that no significant error remains once convergence is achieved.

3.4.6 NOISE CONSIDERATIONS

The thermal noise of a SC integrator as the one targeted in this work is derived in[7] for a conventional differential pair amplifier. The assumption remains valid for the proposed topology since the first stage is still a differential pair, and the input-referred noise of the second stage is reduced by the gain of the first stage, rendering it negligible. The total noise for both phases is thus

$$\overline{v_n^2} = \left(\frac{2kT}{C_1}\right)\left(2+\frac{\gamma_{amp}-1}{1+g_m R}\right), \tag{3.1}$$

with

$$\gamma_{amp} = \gamma\left(1+\frac{g_{m3}}{g_{m1}}\right), \tag{3.2}$$

where γ is a device-dependent fitting parameter with a theoretical value of 2/3, k the Boltzmann constant, T the absolute temperature in kelvin, g_m the transconductance of the differential pair, R the resistance of the switch and g_{m1} and g_{m3} respectively the transconductance of M_1 and M_3. Therefore, to ensure low noise, g_{m3} should be considerably lower than g_{m1}. Biasing the input NMOS in subthreshold guarantees the highest g_{m1} for a given current. As the NMOS is in the same differential pair as the PMOS, it carries the same biasing current and it is therefore sufficient to bias M_3 in moderate inversion to obtain $\gamma_{amp} \approx 1$. The input-referred noise then

reduces to

$$\overline{v_n^2} = \frac{4kT}{C_1}. \tag{3.3}$$

3.5 EXAMPLE DESIGN IN CMOS 65 NM

3.5.1 DESIGN

The proposed rail-to-rail low power dynamic amplifier was initially developed for use in a SC integrator for a ΔΣ ADC. The targeted ADC is a 2+2 LNC-SMASH with a noise-shaping SAR second stage[9]. An amplifier design that meets requirements for the first integrator of the SC loop filter will be presented here. The design is realized using the TSMC 65 nm PDK at 1 V supply.

The target SNR is 90 dB, while the design is thermal noise limited as the SQNR is in excess of 100 dB with an oversampling ratio of 20. The sampling frequency is 20 MS/s, with 10 ns allowed for the amplifying phase and another 10 ns for the sampling phase (the rest of the time is allowed for the second stage noise-shaping SAR).

Maintaining a 3 dB margin, the thermal noise limit is given by

$$\overline{v_n^2} = \frac{V_p^2/2}{10^{\frac{SNR}{10}}}, \tag{3.4}$$

which yields $(11\ \mu\text{V})^2$. Using (3.3), the minimum required capacitor is computed to be 6.8 pF. Dynamic range scaling is added as high-level simulation conducted in [13] indicates an output swing of 80 mV. Rail-to-rail functionality of the amplifier is highly beneficial as dynamic range scaling allows for significant reduction of the feedback capacitors and total output noise. Full swing of 1 V allows for a dynamic range scaling of 8, yielding C_2 of 0.85 pF.

Gain requirements are declined in 2 criteria. Finite gain will result in errors in the transfer function of the modulator and in dead zone preventing small input resolution. Both criteria are explained in [7] and are expressed as the following :

$$A > \frac{OSR}{\pi}\frac{C_1}{C_2} - 1, \tag{3.5}$$

$$A > \sqrt{\frac{p}{\delta}}, \tag{3.6}$$

where OSR is the oversampling ratio, p the amplitude of the recurring pattern when the input is grounded (determined by high-level simulation) and δ the dead zone. The design aims to ensure a dead zone smaller than 10 μV and 3 dB SQNR loss, resulting in a minimum gain requirement of 43 dB. This requirement aligns with previous analysis of 2-stages SMASH $\Delta\Sigma$ ADC[64].

The variable current needed form the variable source has been determined in simulation to yield the required 10 ns settling with as low total power consumption as possible.

3.5.2 SIMULATION RESULTS AND COMPARISON WITH STATIC AMPLIFIER

Fig. 3.5 shows the step response of the proposed amplifier in comparison with an equivalent statically-biased amplifier and the same statically-biased amplifier with a static compensation. Although all responses are nearly identical, the fully static amplifier needs a 460 μA bias current for satisfactory slewing in the first stage. Removing compensation during the amplification phase allows an impressive bias current reduction to 70 μA while keeping the same slewing as no compensation capacitor slows down the amplifier. Finally, the proposed amplifier with the switched compensation and the dynamic bias current allows for variation from 80 μA to 35 μA and from 120 μA to 60 μA for the first and second stage

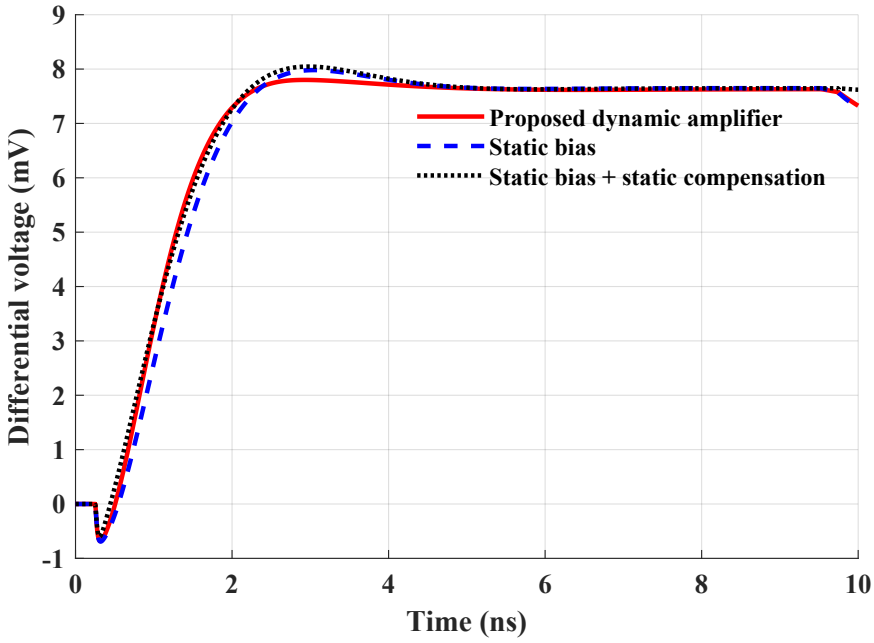

FIGURE 3.5 : Step response comparison between the proposed dynamic amplifier and an equivalent static-current and static-compensation amplifier during the amplification phase. The response is similar, yet the proposed amplifier cut the power consumption in more than half in comparison with the static compensation case and further improves by 20% from the static bias case. Reprinted from [10], © 2024 IEEE.

bias current respectively. Table 3.1 summarize the comparison of the proposed amplifier with the equivalent static designs. The proposed switched compensation allows 2.6 times power consumption reduction while the dynamic biasing further reduces power consumption by 20% for the same 6 τ settling time of 4.9 ns. All amplifiers exhibit a sufficient DC gain of 50 dB meeting all requirements with a comfortable margin for parasitics and process variations in a forthcoming fabricated prototype.

Fig. 3.6 shows the ramp response of the SC integrator presented in Fig. 3.1 incorporating the proposed dynamic amplifier. The transient response shows excellent tracking of the ideal output when taking into account the finite 50 dB gain of the amplifier, which necessarily

causes leakage in the SC since the input can't be at perfect virtual ground and C_1 loses charges due to the non-zero input voltage[188]. The rail-to-rail output stage is shown in action, where error only starts to manifest significantly at 925 mV swing due to the output transistors starting

TABLEAU 3.1 : COMPARISON OF THE PROPOSED DYNAMIC AMPLIFIER WITH EQUIVALENT STATIC AMPLIFIER DESIGNS. REPRINTED FROM [10], © 2024 IEEE.

Design	Proposed	Static bias current	Static bias current and compensation
Open-loop DC gain (dB)	**48.9-49.3**	49.3	49.1
6 τ settling time (ns)	**4.9**	4.9	4.9
Power consumption (μW)	**239**	287	770

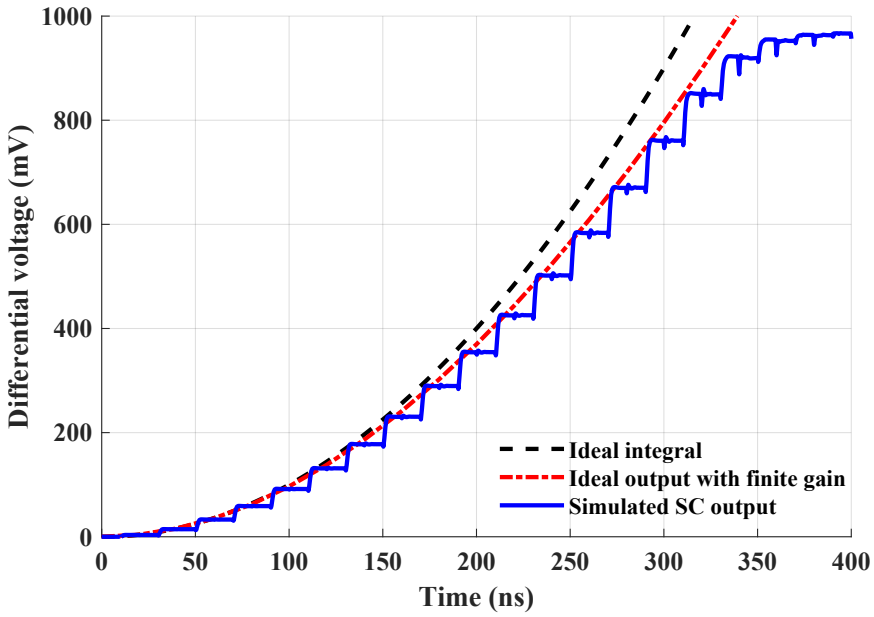

FIGURE 3.6 : Ramp input transient response of the SC integrator incorporating the proposed dynamic amplifier. The maximum output swing reaches 975 mV on a 1 V supply. Reprinted from [10], © 2024 IEEE.

to exit the saturation region. As such, the maximum integrator output is determined to be 975 mV swing.

3.6 CONCLUSION

To conclude, this work introduced a novel rail-to-rail low power dynamic amplifier that is exceptionally well-suited for performing discrete-time filtering in high-precision oversampling ADC. The proposed design leverages a switched compensation scheme to minimize capacitive loading and employs a dynamic biasing scheme to limit power consumption while maintaining fast settling speed. Simulations show a power reduction by 3.2 times compared to a comparable static biasing amplifier, along with accurate integration across more than 90% of the entire rail-to-rail swing.

CHAPITRE IV

A 500 KHZ-BW, 90 DB-SNDR LEAN NOISE-CANCELING SMASH DELTA-SIGMA ADC IN 65 NM CMOS

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4.1 RÉSUMÉ EN FRANÇAIS

Ce papier présente une nouvelle architecture d'ADC ΔΣ conçue pour rencontrer des spécifications exigeantes pour un haut SNDR sur une bande passante modérée. Basée sur un ΔΣ sturdy MASH avec un NS-SAR comme deuxième étage, l'architecture annule le bruit de quantification grâce à la propriété de feedfoward du NS-SAR. L'étage NS-SAR bénéficie aussi d'une réduction significative des contraintes de conception par la filtration additionnelle fournie par le premier étage, permettant une conception très efficace en puissance. Un amplificateur dynamique innovant est proposé pour optimiser les compromis de conception dans le premier intégrateur du circuit. Les résultats de simulation démontrent d'excellentes performances, atteignant 500 kHz de bande passante et 90.3 dB de SNDR avec une consommation de puissance de 1.633 mW, résultant en une FOM_{Sc} de 175.2 dB.

4.2 ABSTRACT

This paper presents a novel ΔΣ ADC architecture designed to meet stringent requirements for high SNDR at moderate bandwidths. Based on a sturdy MASH ΔΣ with NS-SAR second stage, the architecture achieves noise cancellation by virtue of the NS-SAR feedforward property. The NS-SAR stage also benefits from significantly reduced design constraints due to the additional noise shaping provided by the first stage, allowing a more power-efficient design. An innovative dynamic amplifier is proposed to optimize the design trade-off in the first integrator. Simulation results demonstrate excellent performance, achieving 500 kHz bandwidth and 90.3 dB SNDR with a power consumption of 1.633 mW, yielding a FOM_{Sc} of 175.2 dB.

4.3 INTRODUCTION

With the growing interest in Internet-of-Things (IoT) applications for healthcare, industry 4.0 and wireless sensor networks (WSN), the demand for high-performance integrated circuits continues to rise. In particular, high-precision, low-power analog-to-digital converters (ADC) are crucial to accurately process the wide dynamic range of sensor signals while meeting stringent power constraints. Successive approximation register (SAR) ADC are the usual choice for such applications due to their compact design and excellent power efficiency [189, 190, 191]. However, as precision demands increase, SAR ADC quickly face limitations due to excessive comparator noise.

For higher accuracy, the ΔΣ ADC is a common choice to make use of noise shaping to improve the SNR [8]. A notable ΔΣ variant, the noise-shaping SAR (NS-SAR) ADC [27], was developed to overcome the limitations of the SAR ADC while maintaining power efficiency. However, at sampling rates in the upper hundreds of kHz, NS-SAR ADC struggle to exceed

a SNDR of 90 dB due to the larger bit count, which slows down operation and limits the oversampling ratio (OSR). Despite featuring sharp noise transfer functions (NTF) and high-order designs, state-of-the-art NS-SAR still fall short of combining a 90 dB SNDR with a moderate bandwidth [30, 39, 40, 43, 57, 95, 102].

Another promising avenue to tackle these tight requirements comprises the multi-stage noise shaping (MASH) [51] and sturdy MASH (SMASH) [64] ΔΣ ADC. These architectures achieve high-order noise shaping without stability issues by using separate lower-order stages, allowing low OSR so as to benefit from power savings or increased bandwidth. SMASH ADC eliminate MASH's tight matching constraints by eschewing digital filters, but require extensive circuitry to process stage outputs, ultimately affecting power efficiency. Additionally, the first-stage quantization error in SMASH does not automatically cancel and often needs mitigation to maintain SQNR, further increasing the complexity of the design. Most SMASH in literature focus on high-bandwidth applications [65, 66, 67, 69, 192], leaving the moderate-bandwidth high-precision space largely unexplored.

In order to overcome the different limitations of NS-SAR and SMASH in achieving 90 dB SNDR at moderate bandwidth, this work proposes a circuit-level implementation of the Lean Noise-Canceling SMASH (LNC-SMASH) ADC first introduced in [9]. It combines a robust discrete-time (DT) ΔΣ first stage with a NS-SAR second stage, leveraging SMASH's high-order NTF and low OSR to maintain high precision at low sampling rate, significantly reducing power consumption. Noise cancellation is achieved through the intrinsic feedforward property of the NS-SAR, which eliminates the need for additional hardware. Power efficiency is further improved by the use of a novel rail-to-rail dynamic amplifier, while passive summation, SAR quantizers and digital combination eliminate the need for summing amplifiers and error-extraction DAC, thus ensuring a compact, lean design.

This paper begins with a system overview of the LNC-SMASH ADC in section 4.4. Section 4.5 details the novel dynamic amplifier used in the first integrator, followed by simulation results in Section 4.6 and conclusion in Section 4.7.

4.4 SYSTEM OVERVIEW

4.4.1 HIGH-LEVEL OVERVIEW

Fig. 4.1 illustrates the high-level block diagram of the dual-stage LNC-SMASH that enables fourth-order noise shaping without stability constraints and allows a low OSR of 20 for reduced power consumption. The transfer function of a SMASH ΔΣ ADC is given by [64] :

$$Y(z) = STF_1 \cdot V_{in}(z) - NTF_1 \cdot NTF_2 \cdot e_2(z) + NTF_1 \cdot (1 - STF_2) \cdot e_1(z). \tag{4.1}$$

Setting a unity STF_2 to cancel the noise of the first quantizer is particularly challenging because

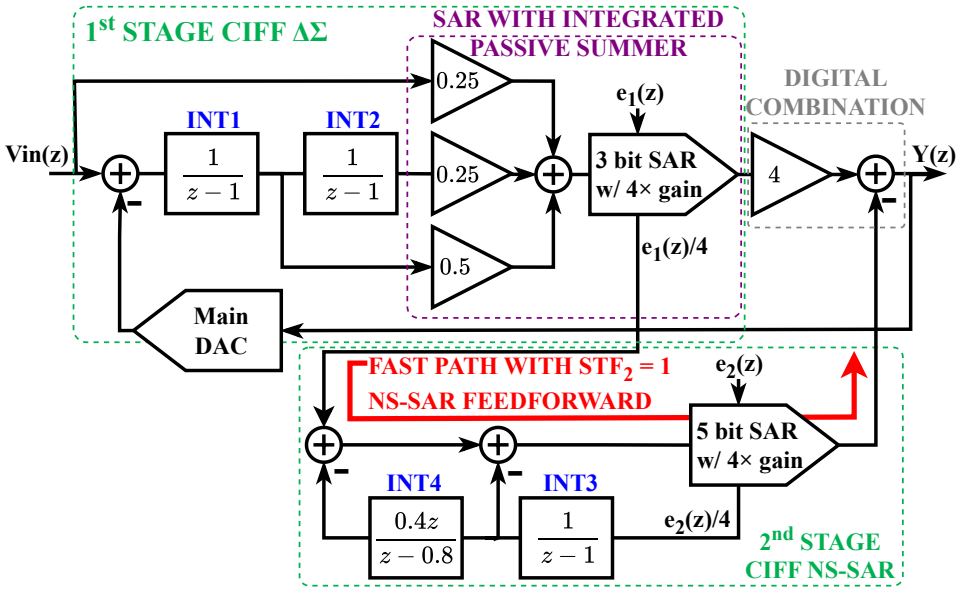

FIGURE 4.1 : Block diagram of the proposed LNC-SMASH ΔΣ ADC. Reprinted from [11], © 2025 IEEE.

the second stage needs to settle before the next sample is taken, resulting in tight timing constraints. As a result, delay blocks or alternate loop configurations are commonly employed in literature [65, 68, 69]. However, the LNC-SMASH, due to the inherent feedforward action of the NS-SAR [28] used as its second stage, not only manages to achieve a unity STF, but also only requires a low bit count SAR quantizer on the signal path. Therefore, it is straightforward to design a SAR quantizer sufficiently fast to meet the timing requirements while yielding a simple, hardware-efficient noise-canceling implementation.

In the proposed circuit presented in Fig. 4.2, the 5-bit SAR uses approximately one third of the conversion period, coordinating well with the first stage operation by slightly extending the sampling phase ϕ_1. The NS-SAR loop filter lies outside the fast signal path, significantly

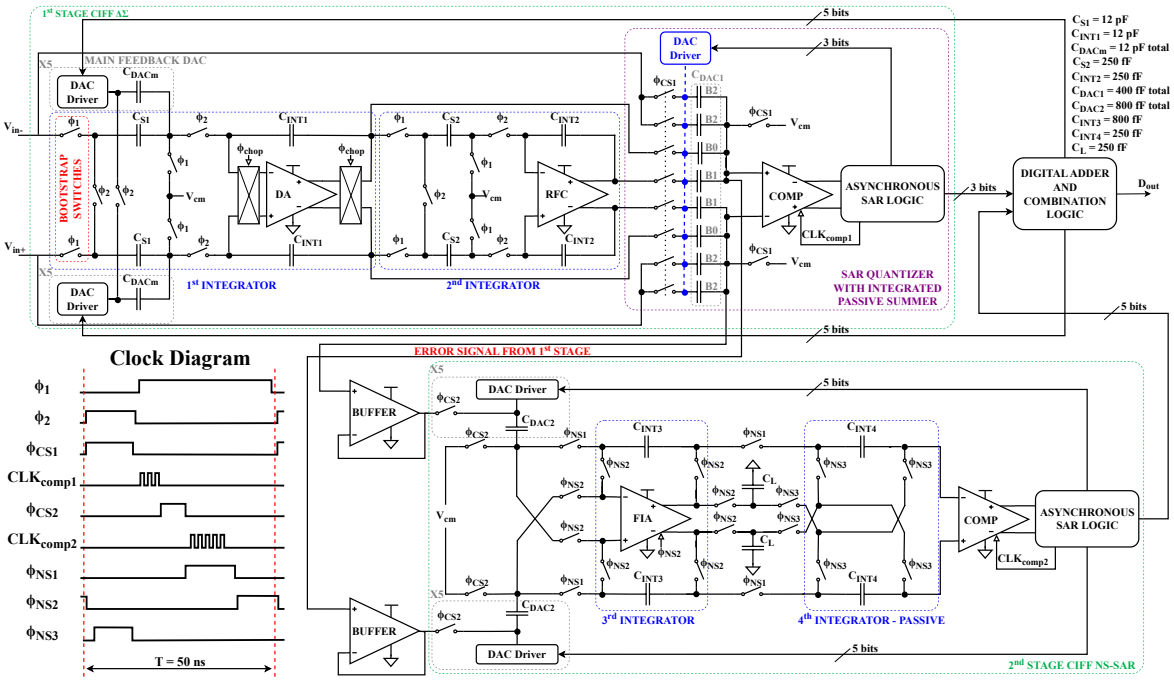

FIGURE 4.2 : Schematic of the simplified implementation of the proposed LNC-SMASH ΔΣ ADC with clock timing diagram. Reprinted from [11], © 2025 IEEE.

easing its timing constraint during ϕ_{NS2} and ϕ_{NS3}. Furthermore, the NS-SAR requires only a low bit count due to the system's high-order noise shaping. Combined with the noise shaping of the first stage, which suppresses NS-SAR's residual DAC and loop errors, and the low swing of the input signal e_1, the design constraints are greatly relaxed, allowing a low-power calibration-free NS-SAR stage. Further analysis of the LNC-SMASH high-level loop structure and comparison with typical MASH and SMASH ΔΣ ADC are presented in [9].

4.4.2 CIRCUIT-LEVEL OVERVIEW

The proposed ADC has a DT ΔΣ first stage with a cascade of integrators with feedforward (CIFF) filter and a SAR quantizer. This structure is selected for its low distortion and relaxed amplifier design constraints, which benefit from reduced signal swing. The first integrator, with the most stringent noise requirements, employs a rail-to-rail low-power dynamic amplifier (DA), which is described in the next section. Bootstrap switches are used for analog signal sampling to limit harmonic distortion [193]. The second integrator employs a recycling folded cascode (RFC) amplifier [194], selected over a conventional folded cascode amplifier for its robustness and enhanced power efficiency.

The first stage quantizer is an asynchronous 3-bit bottom-plate-sampling SAR, where the capacitor array is also repurposed to serve as a passive summer, bypassing the need for a power-hungry summing amplifier. Each capacitor in the SAR DAC array samples a voltage from different circuit nodes, with the resulting sampled voltage representing a weighted sum, determined by the ratio of the sampling capacitor to the total capacitance of the array. To compensate for the fourfold attenuation, the SAR voltage reference is set to one quarter of the supply voltage, effectively restoring the original signal level. At completion of the SAR operation, the first-stage error is extracted through two buffer amplifiers to be fed into the second stage. These buffers use Monticelli class AB op amps [21, 195] to provide high output

drive while maintaining a relatively high gain. Using the buffers to ensure unity gain between the stages and unity STF_2 is essential for minimizing quantization noise leakage, as evidenced by Eq. (4.1).

The first-stage error signal is then quantized by the CIFF NS-SAR second stage. To maintain consistent scaling, the same reference voltage is used as for the SAR of the first stage. The CIFF architecture is selected for its robustness against PVT variations. Instead of the power-hungry multi-input comparator typically required in this structure, the integrator outputs are efficiently summed using a capacitor stacking technique [96]. The NS-SAR loop filter employs a hybrid active/passive topology, combining a floating-inverter amplifier [101] with a passive switched-capacitor integrator that provides 2× gain [95].

Both stage outputs are combined by a digital circuit that applies proper scaling and subtraction. The main feedback DAC is a simple 5-bit binary-weighted capacitor array. The general architecture of the ADC is designed so that the matching constraints are limited exclusively by this DAC, which can be canceled by using foreground calibration, either at startup or periodically during operation [164].

4.5 LOW-POWER RAIL-TO-RAIL DYNAMIC AMPLIFIER

4.5.1 DESIGN CONSTRAINTS FOR THE FIRST INTEGRATOR'S AMPLIFIER

The first integrator is the primary contributor to the thermal noise, since its gain suppresses the input-referred noise of the subsequent stages. Transient noise simulation shows that achieving 90 dB SNR at 20 OSR requires 12 pF sampling capacitors to limit noise on the first integrator, imposing a high capacitive load on the amplifier. In addition, the amplifier must meet strict settling time and open-loop gain requirements to minimize SQNR degradation.

While such amplifiers can be designed, their high static power consumption is a major drawback. A promising solution is the charge-steering dynamic amplifier (DA) [38, 142, 143], which eliminates static bias current for improved efficiency. However, as noted in [142], these DA topologies suffer from variable output common-mode voltage and PVT sensitivity, requiring calibration. The floating-inverter amplifier (FIA) [101] addresses these issues but lacks drive strength and swing due to its finite charge reservoir. Driving a 12 pF load using a FIA would require an impractically large reservoir capacitor, making it highly costly and area-inefficient.

4.5.2 PROPOSED DYNAMIC AMPLIFIER TOPOLOGY

To achieve a better trade-off between high drive capability, compact footprint, and low static power consumption, this work proposes a novel hybrid amplifier balancing static and dynamic operation, based on [10]. The topology, shown in Fig. 4.3 with simplified waveforms, combines a differential pair input stage with a rail-to-rail class AB output stage for strong drive capability. The bias current of the amplifier is dynamically adjusted using a variable ratio current mirror, which acts as a variable current source. At the start of the amplification phase ϕ_2, the current is high for fast slewing. As the amplification phase progresses, less current is required for linear settling. Capacitor C_I ensures a smooth transition between the high-current slewing phase and the low-current linear settling phase. This dynamic approach significantly reduces power consumption during the sampling phase as well, improving overall efficiency.

The bias current of the output stage is controlled by current-based common-mode feedback (CMFB), which sets the bias voltage of the first-stage PMOS active load $M_{3,4}$ via the current branch $M_{17,19}$. The drain current of M_{17}, proportional to the output bias current, is matched to a copy of the variable current source from the current mirror ($M_{16,18,19}$) by the

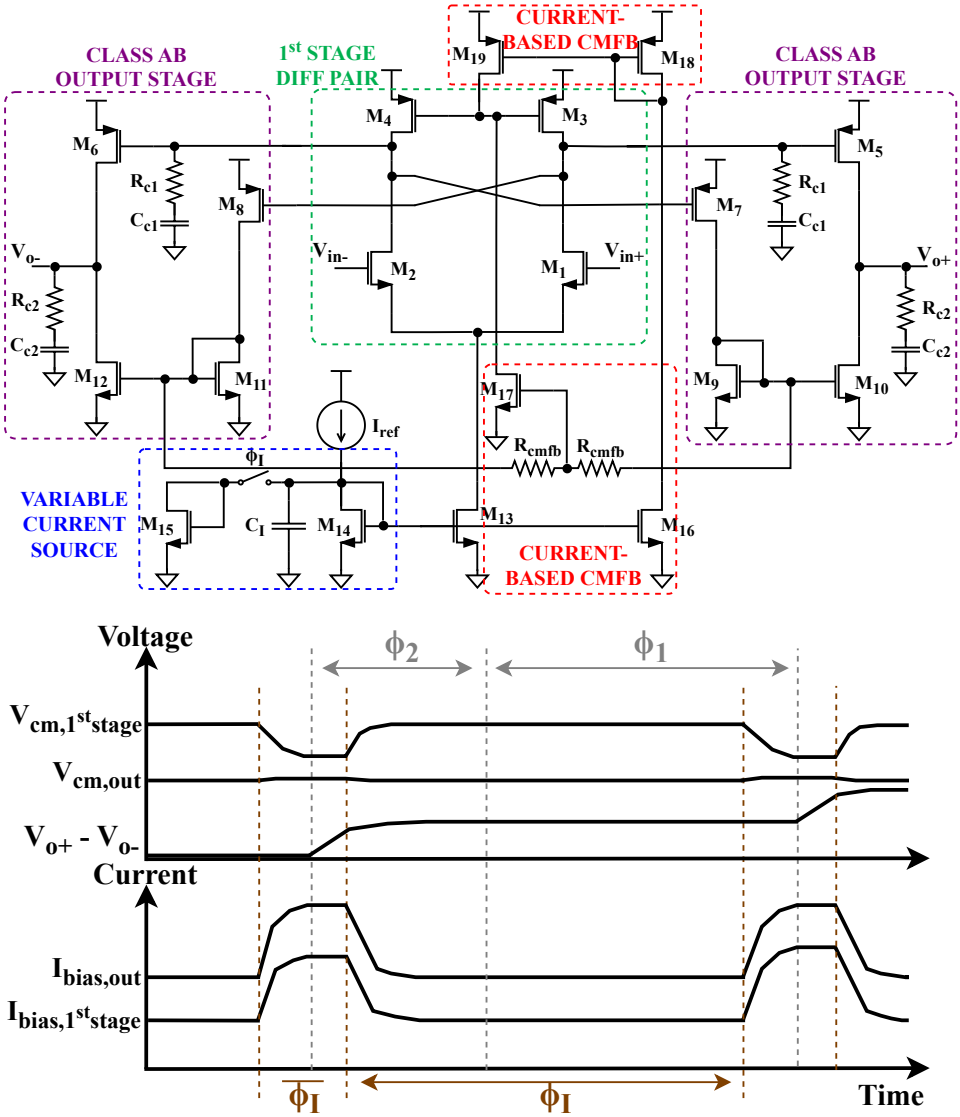

FIGURE 4.3 : Schematic of the proposed rail-to-rail dynamic amplifier with simplified waveforms. Output voltage CMFB omitted for clarity. Reprinted from [11], © 2025 IEEE.

feedback circuit. Another CMFB loop, not shown in the figure, maintains a constant output common-mode voltage[21].

The current-based CMFB improves upon the original design in [10], which relied on a simple buffer as the CMFB element. The present approach provides greater flexibility, allowing independent control of both amplifier stage bias currents, thus enhancing power efficiency.

Additionally, the solution exhibits strong PVT robustness. The output bias current is regulated by the current-mode CMFB, ensuring accuracy solely through device matching ($M_{14,15}$-M_{16} and M_{17}-M_9). Simulations show a 35% reduction in power consumption compared to a statically biased version, dropping from 1.41 mW to 925 μW while maintaining the same transient response time.

4.6 SIMULATION RESULTS

The proposed ADC was designed using a 65 nm standard CMOS process with 1 V supply voltage. To get accurate SNR and SNDR estimations, the simulations incorporate transient noise modeled from the foundry process. Fig. 4.4 presents the simulation results for the power spectral density, where an SNDR of 90.3 dB and SFDR of 105.1 dB are achieved, demonstrating the high precision of the fourth-order LNC-SMASH architecture. The minimal

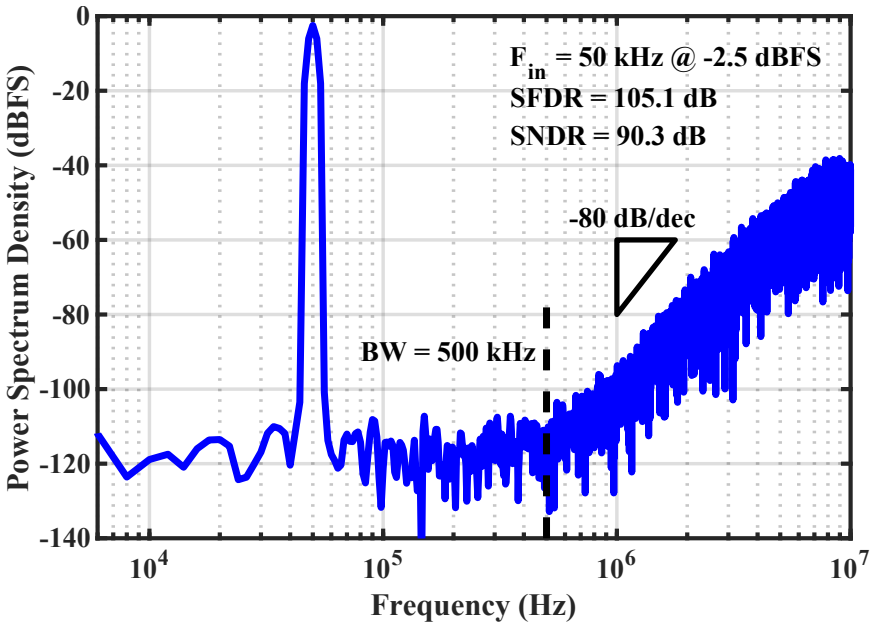

FIGURE 4.4 : Simulated power spectrum density of the proposed ADC. Reprinted from [11], © 2025 IEEE.

harmonic peaks in the response highlight the low distortion of the circuits, attributed to the low-swing topology used.

Fig. 4.5 shows the SNR and SNDR as functions of input amplitude. Distortion remains very low, with the SNDR closely tracking the SNR curve up to an input level of -2 dBFS. The dynamic range is 95.4 dB.

Fig. 4.6 depicts the simulated power breakdown of the LNC-SMASH. As expected, the first integrator is the most power-hungry circuit, consuming more than half of the total power budget. The NS-SAR second stage, with its relaxed constraints, consumes only 50 μW while significantly contributing to improve the overall SQNR. Despite the necessary buffer to minimize quantization noise leakage, the total additional power consumption of the second stage remains below 25% of the ADC total power consumption of 1.633 mW.

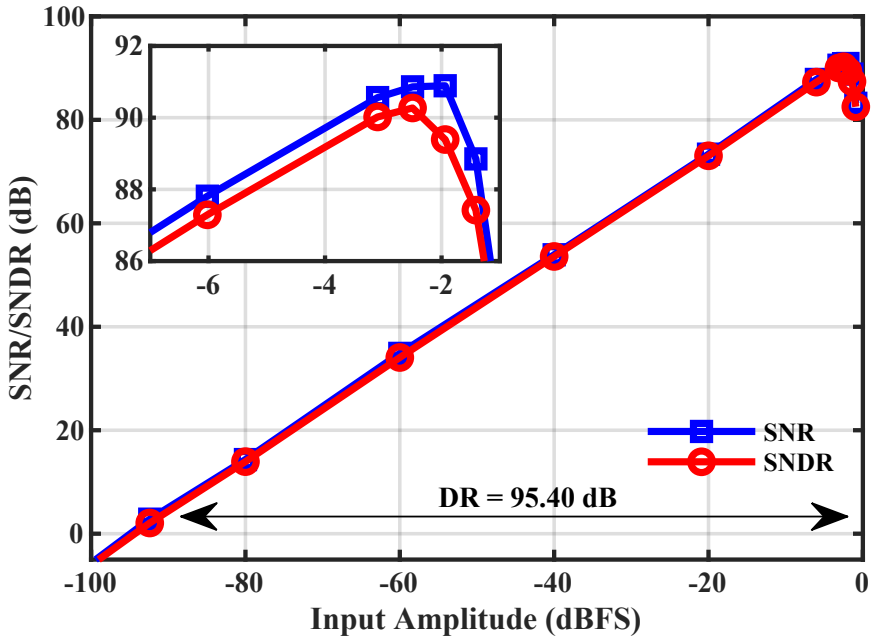

FIGURE 4.5 : Simulated SNR and SNDR as functions of input amplitude for an input signal of 50 kHz. Reprinted from [11], © 2025 IEEE.

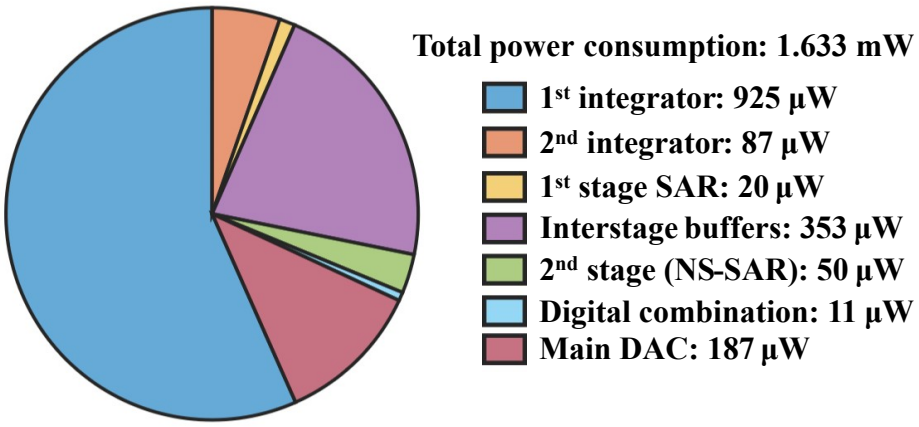

FIGURE 4.6 : Power distribution for the stages of the proposed ADC (simulated). Reprinted from [11], © 2025 IEEE.

Table 4.1 compares the performance of this LNC-SMASH to other state-of-the-art ΔΣ ADC. Since the proposed ADC is only simulated for now, it may be somewhat advantaged over measured state-of-the-art implementations, as performance could slightly degrade under real-world conditions. Nevertheless, as the only design to reach 90 dB SNDR at 500 kHz bandwidth and above, the LNC-SMASH stands out as highly competitive. Although LNC-SMASH unsurprisingly lags behind NS-SAR's power consumption, it remains remarkably power efficient compared to other SMASH implementations.

4.7 CONCLUSION

In conclusion, this work presents the LNC-SMASH ΔΣ ADC, utilizing the NS-SAR's feedforward property for efficient noise cancellation. The dual-stage design relaxes NS-SAR constraints, enhancing hardware and power efficiency. A novel DA optimizes balance between drive strength, area, and power consumption for the first integrator. The simulated ADC demonstrates excellent performance compared to state-of-the-art SMASH architectures,

TABLEAU 4.1 : PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART ΔΣ ADC. REPRINTED FROM [11], © 2025 IEEE.

	This work	[64]	[192]	[95]	[39]
Architecture	**LNC-SMASH**	SMASH	SMASH	NS-SAR	NS-SAR
Meas./sim.	**Sim.**	Meas.	Meas.	Meas.	Meas.
Process	**65 nm**	180 nm	65 nm	40 nm	65 nm
Supply (V)	**1**	1.2	1.1/1.3	1.1	1.2/2
Power (μW)	**1633**	3300	12500	340	73.8
F_s (MS/s)	**20**	20	500	5	5
OSR	**20**	16	16	10	5
BW (kHz)	**500**	625	15625	250	500
SNDR (dB)	**90.3**	74.6	74	93.3	84.1
SFDR (dB)	**105.1**	89.7	84.2	104.4	97
FOM_{Wa}	**61.0**	601.5	97.7	18.0	5.6
FOM_{Sc}	**175.2**	157.4	165.0	182.0	182.4

$FOM_{Wa} = Power/(2^{ENOB} \cdot F_s)$ $[fJ/conv.-step]$
$FOM_{Sc} = SNDR + 10 \cdot log(BW/Power)$ $[dB]$

offering a power-efficient solution capable of 90 dB SNDR at hundreds of kHz, a stringent specification that is likely to grow in relevance along the developing applications landscape.

CHAPITRE V

ROBUSTESSE AUX VARIATIONS ET COMPARAISON AVEC L'ÉTAT DE L'ART

Ce dernier chapitre complètera les articles présentés jusqu'à présent dans ce mémoire avec des résultats de simulations supplémentaires démontrant le bon fonctionnement du LNC-SMASH sur les variations PVT. Une comparaison plus complète pour bien situer l'ADC conçu avec l'état de l'art sera aussi présentée.

5.1 ROBUSTESSE AUX VARIATIONS PVT

Pour s'assurer du bon fonctionnement de l'ADC en condition réelle, il est important de vérifier si les performances nominales en simulation ne sont pas trop dégradées en présence de variations de procédé, de température et de tension d'alimentation. D'abord, pour les températures, la Fig. 5.1 présente les résultats de simulations de la variation du SNR et du SNDR pour un changement de -10°C à +70°C. La dégradation maximale du SNR est de 1.6 dB à -10°C alors que la dégradation maximale de SNDR est de -3.2 dB 70°C en raison de la troisième harmonique qui pointe davantage à cette température. Probablement que certaines parties du circuit deviennent trop rapides à haute température et certaines tensions de polarisation auraient besoin d'ajustements. Les performances restent satisfaisantes.

Pour le voltage, les cas à ±5% de l'alimentation nominale de 1 V ont été testés. Cela représente une plage amplement suffisante parce que l'alimentation d'un ADC est toujours réglée avec un régulateur linéaire à bas bruit et haute précision pour éviter les grandes variations d'alimentation. Les résultats de la variation du SNR et du SNDR sont montrés à la Fig. 5.2. Le circuit est peu sensible aux variations de tension avec tous les résultats à l'intérieur de ±1 dB de variation.

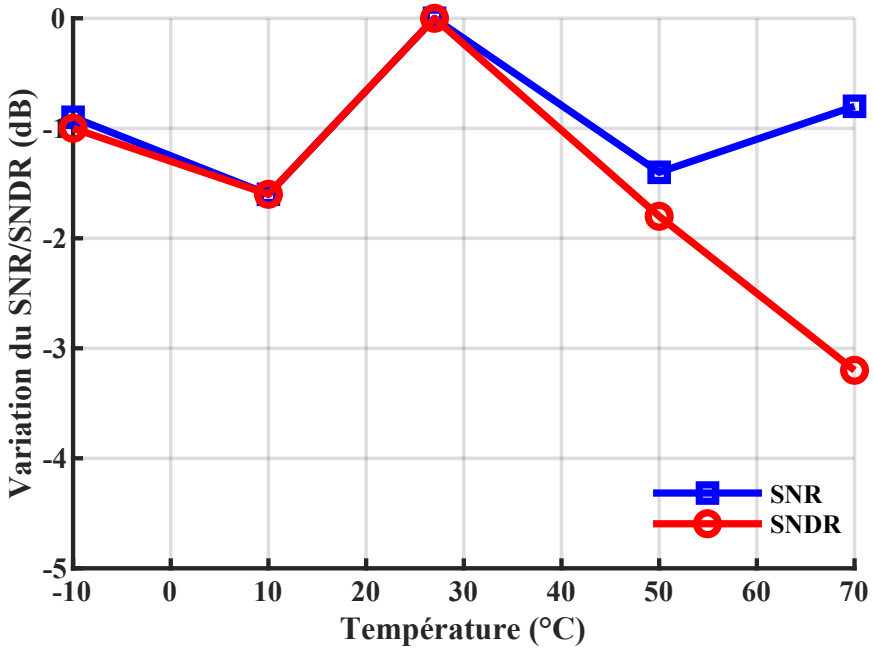

FIGURE 5.1 : Simulation de la variation du SNR et du SNDR en fonction de la température.

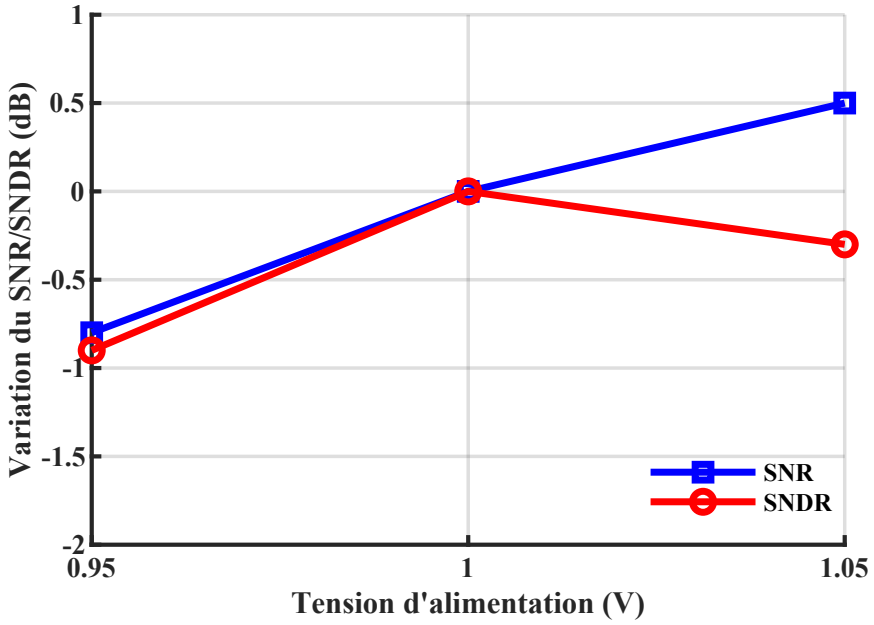

FIGURE 5.2 : Simulation de la variation du SNR et du SNDR en fonction de la tension d'alimentation.

Finalement, pour les variations de procédés, des simulations incluant les modèles de variations de procédé et de mismatch de la fonderie ont été effectuées. On réalise généralement ces simulations sous forme de simulation Monte Carlo de 50 échantillons ou plus pour avoir une représentation statistique adéquate des variations des modèles selon la loi normale. Cependant, le modèle transistor de l'ADC complet doit simuler pour 10k points, ce qui demande environ une dizaine d'heures de simulation. Deux simulations sont nécessaires pour chaque échantillon : un ton hors bande pour calibrer les mismatch dans le DAC et un ton dans la bande pour tester l'ADC. Il est donc prohibitivement trop long de faire une analyse Monte Carlo digne de ce nom. Ainsi, seulement 5 échantillons aléatoires ont été simulés. Les résultats des 5 échantillons sont tracés dans la Fig. 5.3. L'échantillon numéro 3 présentait déjà des performances supérieures à ce que la calibration pouvait améliorer. L'échantillon numéro 5 est très mauvais au départ car en plus des variations de mismatch de la fonderie, un des éléments du DAC principal a été réduit de 375 fF à 350 fF pour représenter un défaut de

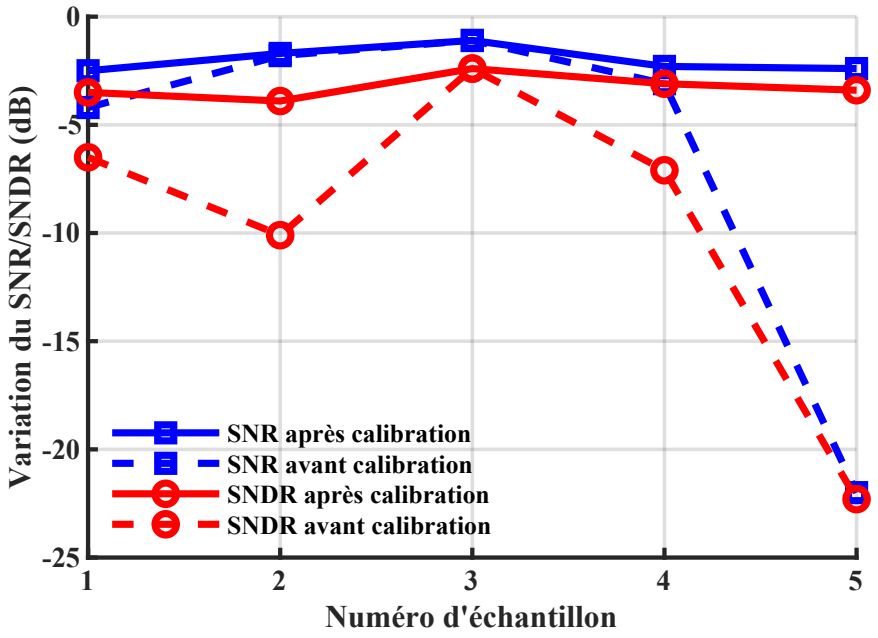

FIGURE 5.3 : Simulation de la variation du SNR et du SNDR pour 5 échantillons incluant des variations de procédé aléatoires.

fabrication ou un cas critique de mismatch. On remarque qu'après la calibration, les résultats sont relativement satisfaisants avec une réduction du SNR autour de 2 dB et du SNDR autour de 3 dB.

On peut conclure que l'ADC est assez robuste en présence de variations PVT, mais on peut s'attendre à perdre la précision nominale de 90.3 dB de SNDR une fois la puce fabriquée pour une valeur réaliste autour de 85 à 88 dB.

5.2 COMPARAISON AVEC L'ÉTAT DE L'ART

La Fig. 5.4 est une reproduction de la Fig. 1.11 présentée dans la revue de littérature. Elle contient les implémentations d'ADC à suréchantillonnage provenant des meilleurs journaux IEEE au courant des 5 dernières années. Le point d'opération correspondant à l'ADC ΔΣ LNC-SMASH a été ajouté avec le rond bleu mis en évidence. On peut voir que l'ADC proposé se classe assez compétitivement par rapport aux autres ΔΣ de l'état de l'art. La FOM_{Sc} du LNC-SMASH est de 175.2 dB ce qui le positionne un peu au-dessus de la moyenne des autres designs, un fait aussi mis en évidence par sa position au centre du nuage de point.

La Fig. 5.5, une reproduction de la Fig. 1.13 en incluant l'ADC proposé, met mieux en évidence la force du LNC-SMASH. Le nuage de points montre l'ENOB en fonction de la bande passante. On peut voir qu'au-dessus de 250 kHz de bande passante, le LNC-SMASH est le seul parmi les meilleurs ADC à suréchantillonnage des 5 dernières années à atteindre un ENOB supérieur à 14 bits. Ainsi, malgré son efficacité énergétique dans la moyenne de l'état de l'art, le LNC-SMASH se démarque en permettant d'atteindre de très hautes performances en termes de précision à bande passante modérée. Cela permet de remplir les spécifications de certaines applications demandantes comme l'imagerie par ultrason, les sonars

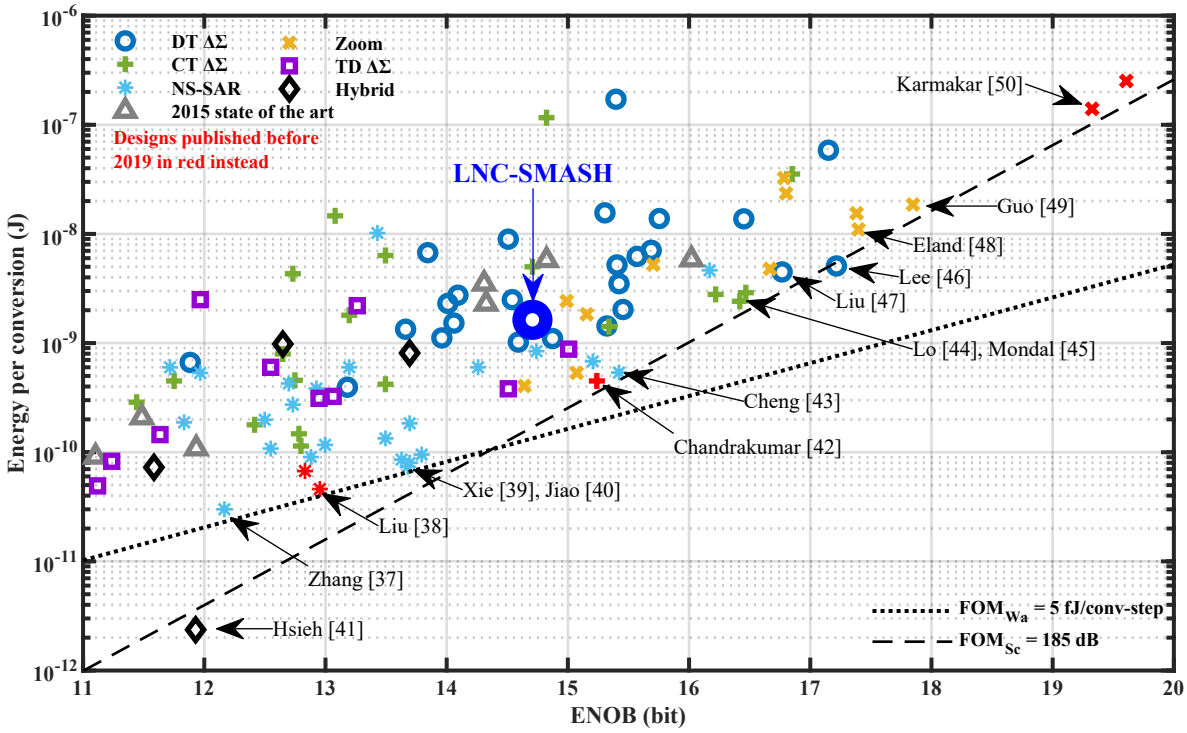

FIGURE 5.4 : Nuage de points montrant le compromis efficacité énergétique/résolution pour les ADC sélectionnés dans la revue de littérature. L'ADC LNC-SMASH proposé est ajouté parmi les points.

ou l'analyse de vibrations, le tout à relativement bonne efficacité énergétique. On note aussi que le LNC-SMASH atteint une bande passante supérieure à tous les DT ΔΣ du graphique.

Il ne faut pas oublier que le LNC-SMASH présente seulement des résultats de simulation alors que tous les autres designs ont des résultats de mesures. On peut donc s'attendre à perdre quelques dB de SNDR et de FOM avec l'implémentation réelle. Néanmoins, on remarque que le LNC-SMASH est très compétitif par rapport aux autres ADC à suréchantillonnage grâce à l'annulation du bruit de quantification très efficace implémentée avec le second étage NS-SAR. La filtration du bruit de quantification d'ordre 4 et l'implémentation efficace du circuit électronique rendent aussi la nouvelle architecture très compétitive.

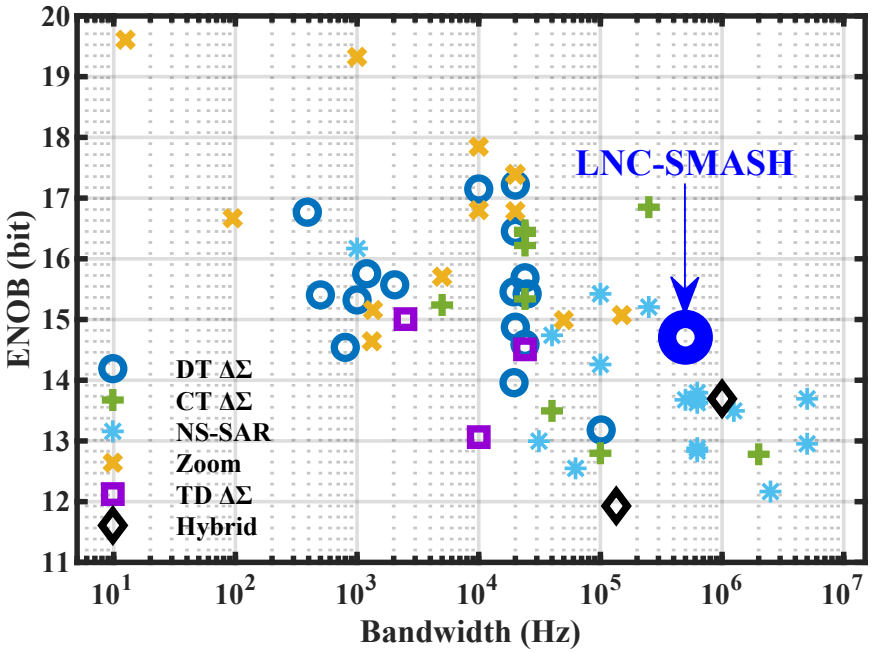

FIGURE 5.5 : Nuage de points montrant l'ENOB en fonction de la bande passante pour les 60 meilleurs designs étudiés (FOM_{Sc} > 172 dB). L'ADC LNC-SMASH proposé est ajouté parmi les points.

CONCLUSION

SYNTHÈSE

Pour conclure, ce mémoire propose une nouvelle architecture d'ADC ΔΣ. La topologie proposée est une amélioration de la topologie SMASH dans laquelle le deuxième étage est stratégiquement remplacé par un convertisseur NS-SAR. Cela permet d'exploiter la propriété de feedforward inhérente à ce type de convertisseurs pour annuler le bruit de quantification du premier étage, améliorant la précision du convertisseur. L'utilisation du NS-SAR en deuxième étage permet aussi de garder son amplitude d'entrée basse, ce qui réduit les contraintes de conception et permet une implémentation très efficace.

Le circuit complet de l'ADC a été conçu au niveau transistor sur Cadence Virtuoso avec la technologie CMOS 65 nm. Différentes techniques ont été utilisées pour maximiser les performances du circuit, notamment l'utilisation d'un amplificateur dynamique permettant un meilleur compromis entre faible consommation de puissance, faible encombrement et capacité d'attaquer de grandes charges. Un sommateur passif réutilisant les condensateurs de la banque du DAC du quantificateur SAR du premier étage est aussi utilisé pour sauver un amplificateur et diminuer la consommation de puissance.

Les résultats de simulation démontrent de très bonnes performances comparables à celles des meilleures implémentations d'ADC à suréchantillonnage de l'état de l'art avec un SNDR de 90 dB et une consommation de puissance de 1.6 mW sur une bande passante de 500 kHz. La force de cette nouvelle architecture est d'atteindre à la fois une haute précision et une bande passante de plusieurs centaines de kilohertz, des spécifications assez contraignantes, tout en conservant une consommation de puissance basse. Cela rend cet ADC parfait pour les applications demandantes comme l'acquisition de données provenant d'ultrasons, des sonars ou de l'analyse de vibrations.

Des simulations étendues couvrant les variations de procédé, de température et de tension d'alimentation ont aussi été conduites pour vérifier la robustesse de l'ADC conçu. Les résultats sont aussi très satisfaisants et montrent une tolérance raisonnable à toutes les variations anticipées. La dégradation des performances est faible et atteint moins de 5 dB de SNDR dans les pires scénarios. La nouvelle topologie est donc robuste et présente un fort potentiel pour la réalisation et la fabrication d'un prototype pour confirmer les performances avec des mesures en laboratoire.

TRAVAUX FUTURS

Afin de poursuivre les recherches présentées dans ce mémoire, la première étape consistera à valider expérimentalement le fonctionnement de l'ADC proposé en laboratoire. Cela impliquera le dessin des masques et la préparation des fichiers nécessaires à la fabrication du circuit avec la technologie CMOS 65 nm. Des simulations incluant les parasites et plusieurs techniques de routage et de placement des transistors devront être mises en oeuvre pour assurer le bon fonctionnement du circuit.

Par ailleurs, plusieurs pistes explorées au cours du projet n'ont pas été retenues dans la version finale, mais restent très pertinentes et pourraient être envisagées pour de futures itérations de l'ADC. Sur le plan architectural, une avenue prometteuse serait de concevoir une structure permettant de fusionner les deux quantificateurs SAR en un seul bloc, ce qui réduirait l'encombrement et la consommation de puissance. De plus, les buffers utilisés pour transmettre le signal d'erreur du premier au deuxième étage pourraient être optimisés, voire éliminés, en repensant la structure de la boucle. Cela permettrait de réduire la consommation de puissance statique significative dans ce bloc.

Enfin, l'une des principales contraintes de conception actuelles réside dans le bruit thermique du premier intégrateur, qui impose l'utilisation de condensateurs d'échantillonnage de 12 pF. Explorer ou développer une technique efficace d'annulation du bruit thermique représenterait une avancée notable pour améliorer les performances globales du circuit.

En terminant, ce mémoire témoigne de la richesse du domaine de la conception d'ADC à suréchantillonnage. La nouvelle topologie proposée ne constitue qu'une pièce du vaste casse-tête formé par la multitude de solutions explorées dans la littérature. De nombreuses avancées restent à venir dans ce domaine en constante évolution, porté par le développement continu des technologies CMOS.

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