A Lean Noise-Canceling SMASH Delta-Sigma ADC in 65-nm CMOS

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***Abstract*—This paper presents a novel $\Delta\Sigma$ ADC architecture designed to simultaneously achieve moderate to high bandwidth and high SNDR. The proposed converter builds on a sturdy MASH $\Delta\Sigma$ topology, where the second stage is replaced by a noise-shaping SAR (NS-SAR). Thanks to the feedforward property of the NS-SAR, the quantization noise of the first stage is effectively canceled. A novel dynamic amplifier is proposed for the first integrator, providing an improved trade-off between area, drive capability, and power consumption. In addition, a passive summation scheme that reuses the quantizer capacitor array is employed, eliminating the need for a power-hungry amplifier. Simulation results demonstrate an SNDR of 89 dB over a 500 kHz bandwidth with a power consumption of 1.73 mW, corresponding to a FOM_{Sc} of 173.7 dB. Extensive simulations further confirm robust stability across PVT variations.**

***Index Terms*—Analog-to-digital converter (ADC), delta-sigma modulator, oversampling, noise-shaping SAR, multi-stage noise shaping (MASH), sturdy MASH (SMASH), dynamic amplifier.**

I. Introduction

THE demand for high-performance analog-to-digital converters (ADC) continues to grow with the rapid expansion of applications in biomedical imaging, industrial monitoring, Internet of Things (IoT) and precision instrumentation. Increasingly, these systems must deliver both wide bandwidth and high signal fidelity, while operating under stringent power budgets to enable portable, battery-powered platforms. Meeting these diverse and often conflicting requirements has proven challenging for conventional ADC architectures.

For embedded applications, successive approximation register (SAR) ADC are typically favored due to their compact form factor and excellent power efficiency [1]–[3]. However, when a high signal-to-noise-and-distortion ratio (SNDR) is required, the SAR ADC faces fundamental limitations arising from comparator noise and large DAC capacitor footprint.

In contrast, $\Delta\Sigma$ ADC excel in high-SNDR applications by virtue of their noise-shaping properties and architectural flexibility [4]. However, achieving high resolution and wide bandwidth remains challenging, as the oversampling ratio (OSR) imposes a fundamental limit on the SNR–bandwidth trade-off. Hybrid approaches such as the noise-shaping SAR (NS-SAR) [5] have demonstrated outstanding figures of merit (FOM) by embedding a SAR quantizer within a noise-shaping loop, enabling great power efficiency even at high precision. Still, as sampling rates approach the upper hundreds of kilohertz, NS-SAR designs struggle to maintain SNDR above 90 dB because of the increased quantizer bit count, which slows conversion and limits the achievable OSR. State-of-the-art implementations still fail to simultaneously achieve moderate bandwidth [6]–[8] and 90 dB SNDR [9]–[12].

A promising alternative lies in multi-stage noise-shaping (MASH) [13] $\Delta\Sigma$ ADC. This architecture cascades multiple low-order $\Delta\Sigma$ modulators to achieve high-order noise shaping without compromising stability, thereby reducing OSR and enabling more favorable bandwidth–power trade-offs. However, stringent matching between stages is required to prevent first-stage quantization noise leakage, which can significantly degrade the output SNDR. To relax these matching requirements, the sturdy MASH (SMASH) architecture was introduced [14]. While SMASH preserves aggressive high-order noise shaping, it sacrifices cancellation of the first-stage quantization noise and exhibits a reduced stability margin in comparison to MASH. Noise-canceling SMASH variants have been proposed, but these typically require additional circuitry or complex loop structures. Furthermore, because of their reduced OSR, most SMASH designs in the literature have targeted high-bandwidth applications [15]–[19], leaving the moderate-bandwidth, high-precision domain relatively unexplored.

To address this gap, this work proposes a circuit-level implementation of the Lean Noise-Canceling SMASH (LNC-SMASH) [20]. The proposed ADC combines a discrete-time (DT) $\Delta\Sigma$ modulator as the first stage with an NS-SAR as the second stage. By exploiting the inherent feedforward property of the NS-SAR, quantization noise from the first stage can be effectively canceled without resorting to complex loop structures or additional hardware. At the same time, the NS-SAR benefits from the noise shaping of the first stage, relaxing its design and matching constraints, and allowing a highly power-efficient implementation. The use of passive summation, SAR quantizers, and digital combination eliminates the need for summing amplifiers, feedback paths, or error-extraction DAC, resulting in a hardware-lean ADC design.

This paper extends the results presented in the original conference proceedings [21] by adding a review of existing noise-canceling SMASH architectures, sections on circuit-level implementation, and results on sensitivity to process, voltage, and temperature variations. It further includes layout considerations, post-layout simulation results, and an expanded comparison with state-of-the-art oversampling ADC designs.

The remainder of the paper is organized as follows. Section II presents the high-level structure of the LNC-SMASH

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and compares it against other noise-canceling SMASH architectures reported in the literature. Section III and IV describe the key circuit innovations, respectively the novel dynamic amplifier and the passive summer. Section V discusses the overall ADC implementation and simulation results. Finally, section VI concludes the work.

II. Background and System-Level Overview

A. Review of the SMASH Architecture

Fig. 1 illustrates the two-stage SMASH $\Delta\Sigma$ ADC architecture. In this topology, the quantization error of the first stage is processed by a second $\Delta\Sigma$ modulator, which refines the overall quantization accuracy. The second stage output, representing the digital equivalent of the first-stage quantization error, is then subtracted from the main signal path to generate the high SNDR output. By keeping the two low-order loops separate, the architecture significantly relaxes the stability constraints compared to a single high-order loop. Unlike the MASH approach, the entire operation is carried out in the analog domain, eliminating the need for tight matching between analog and digital paths. This reduces the op-amp gain requirements needed to achieve proper error cancellation [14]. The overall transfer function is expressed as:

$$Y(z) = STF_1 V_{in}(z) - NTF_1 NTF_2 e_2(z) + NTF_1(1 - STF_2)e_1(z), \quad (1)$$

where STF_n and NTF_n denote the signal and noise transfer functions of the nth stage of the SMASH ADC, respectively. Typically, STF_2 is selected such that $STF_2 = 1 - NTF_2$, ensuring that the quantization noise from both stages is shaped by the same high-order noise transfer function.

Most state-of-the-art SMASH $\Delta\Sigma$ ADC target high-bandwidth applications [15]–[19], with sampling rates limited to approximately 1–2 GS/s. At these speeds, the transistor frequency limit makes it difficult to achieve the required specifications within the loop filter, quantizer, and DAC circuits. The aggressive noise shaping of SMASH enables a reduced OSR, making this architecture well suited for maximizing usable signal bandwidths on the order of several tens of megahertz.

This work instead leverages SMASH's low-OSR property in the low-frequency regime to minimize the sampling rate for a given bandwidth, reducing power consumption. However, achieving high precision through SMASH presents several challenges. Since the first-stage quantization noise is not canceled, identical quantizer resolutions are required in both stages, increasing circuit complexity and still imposing an inherent 6 dB signal-to-quantization-noise ratio (SQNR) penalty. Noise-canceling SMASH variants that attempt to mitigate these issues are discussed in the next section.

B. Review of Prior Noise-Canceling SMASH Architectures

Noise cancellation is a powerful technique to enhance SMASH performance, as it allows the use of a lower-resolution first-stage quantizer without compromising overall ADC accuracy. This reduction in bit count translates directly into lower

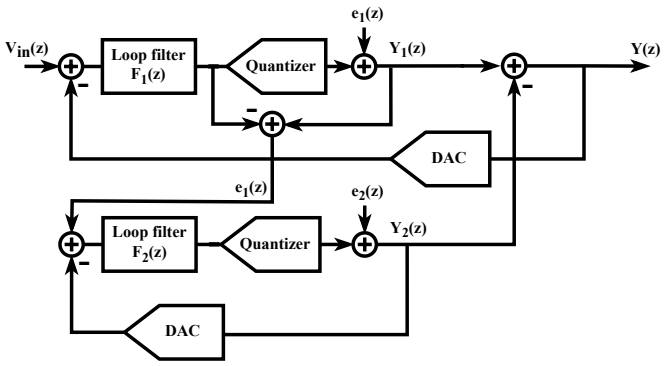

Fig. 1. Block diagram of the SMASH $\Delta\Sigma$ ADC.

circuit complexity and power consumption. A straightforward approach would be to set STF_2 to unity in Eq. (1), thereby enabling direct noise cancellation. However, this solution is challenging to realize in practice, as it requires the second stage to produce an accurate estimate of the first-stage quantization error within a single sampling interval, introducing very tight timing constraints.

To address these stringent timing requirements, several solutions have been proposed in literature. For instance, Han [22] introduced a delay-based method illustrated in Fig. 2(a). By inserting a delay in the signal path, the second stage is given additional time for processing, and the subtraction of the two stages can be carried out in the following sampling period while implementing noise cancellation. However, to maintain modulator stability under this scheme, an additional fast feedback loop around the first-stage quantizer is required. Depending on the specific implementation, this auxiliary feedback path may involve a power-hungry full scale summing amplifier and an additional DAC, increasing circuit complexity.

Next, as shown in Fig. 2(b), Yoon [15] proposed a continuous-time (CT) implementation of the SMASH architecture that achieves noise cancellation. Similarly to the previous approach, this method introduces additional delays to provide the second stage with more processing time. In this case, however, the delays are implemented in the analog domain. To reduce power consumption, the design employs low-pass filters instead of sample-and-hold circuits, which would be prohibitively power-hungry. While effective, this solution not only adds circuitry, but is also sensitive to delay matching and suffers from STF peaking.

Another solution was presented in [16] and is illustrated in Fig. 2(c). This resolution-enhanced SMASH achieves noise cancellation by inserting a half-delay block before the first quantizer and rearranging the loop structure to relax both timing and stability constraints. To limit circuit overhead, a DAC sharing technique is employed. Nevertheless, the architecture requires multiple additional summing nodes, which must be implemented either with passive summing networks followed by gain stages to compensate for attenuation or with power-hungry active summing amplifiers.

C. Proposed LNC-SMASH Architecture

The proposed LNC-SMASH architecture is illustrated in Fig. 3. In this design, the second stage of the conventional

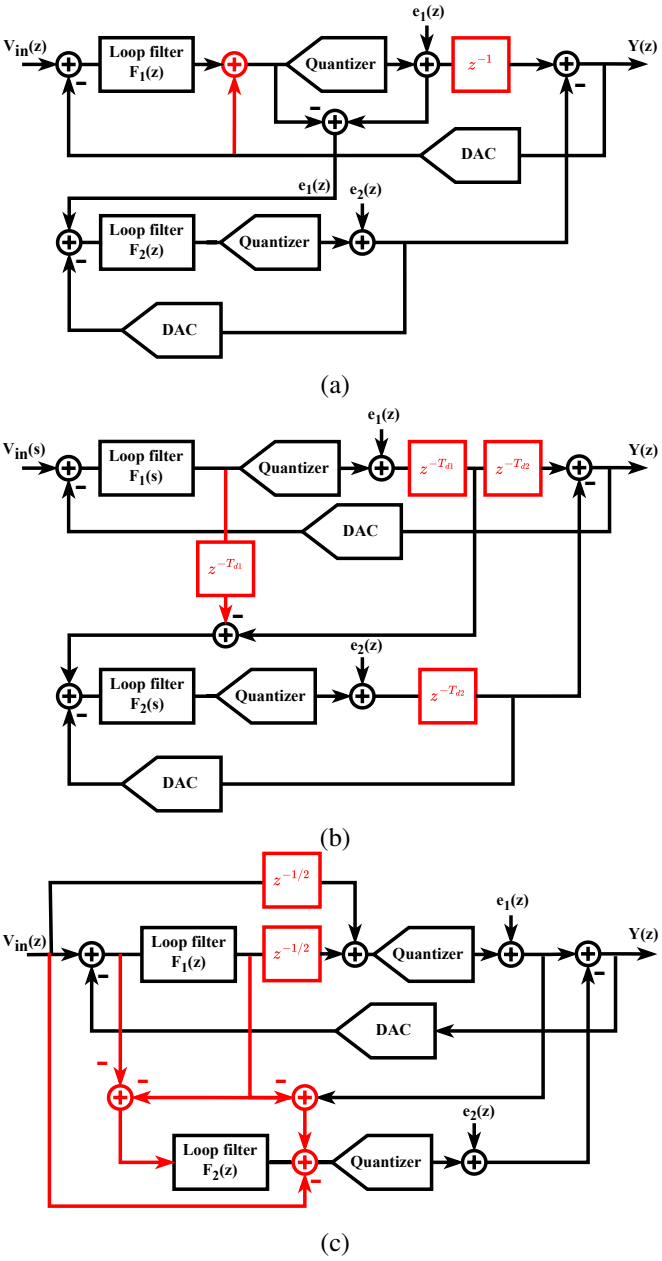

Fig. 2. Prior noise-canceling SMASH $\Delta\Sigma$ ADC architectures highlighting in red deviations from the conventional SMASH configuration: (a) delay-based noise canceling, (b) CT SMASH, and (c) resolution-enhanced SMASH.

SMASH structure is strategically replaced by a noise-shaping SAR (NS-SAR) ADC. Thanks to its inherent feedforward property [23], the NS-SAR achieves a unity STF, which directly enables noise cancellation. Furthermore, because the NS-SAR holds its loop filter inside the feedback path, the main signal path of the second stage remains clear of filtering elements, leaving only a low bit count SAR quantizer. This configuration makes it relatively straightforward to implement a fast path through the second stage: as long as the SAR quantizer operates quickly enough, its output can be subtracted from the first-stage output before the next sampling instant, thereby achieving noise cancellation.

It is worth noting that the proposed noise-canceling architecture can, in principle, be implemented using any DT

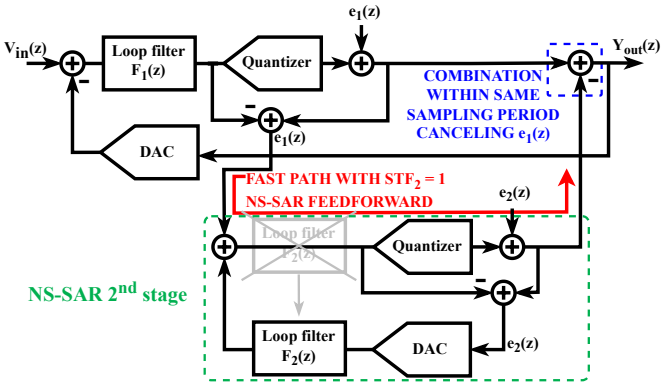

Fig. 3. Block diagram of the proposed LNC-SMASH $\Delta\Sigma$ ADC, where the second stage is replaced by a noise-shaping SAR (NS-SAR) to enable noise cancellation.

$\Delta\Sigma$ ADC topology, provided that the STF is unity. For example, a general second-order modulator with an input feedforward path similar to that of the first stage could be used. However, a key drawback of this approach would be that the loop filter operations lie within the critical fast path, imposing stringent settling requirements on the integrators and consequently increasing their power consumption.

Moreover, NS-SAR ADC are also well known for their excellent power and area efficiency, with numerous designs reported to demonstrate strong performance at moderate resolutions and relatively high bandwidths [24], [25]. These characteristics make the NS-SAR particularly well suited as the second stage in SMASH, where it processes only a fraction of the overall noise-shaping but must do so rapidly in order to satisfy the timing constraints. At the design level, the NS-SAR also benefits from relaxed circuit constraints. Specifically, the feedback DAC and loop filter non-idealities of the NS-SAR, which are typically not noise-shaped by the modulator, are now shaped by the first-stage NTF. As a result, the proposed architecture provides a lean and efficient realization of noise cancellation in SMASH without requiring additional hardware.

Simulation results presented later in this work confirm that allocating approximately one third of the clock period to the NS-SAR fast path is sufficient, requiring only minor speed improvements in the first stage. It is important to note that the NS-SAR loop filter is not part of the fast signal path, which leaves its timing requirements relaxed.

Although the proposed LNC-SMASH ADC may resemble prior SAR- or NS-SAR-assisted $\Delta\Sigma$ ADC, it differs fundamentally. Conventional SAR-assisted $\Delta\Sigma$ ADC [26], [27] rely on noise coupling for high-order noise shaping, whereas NS-SAR-nested $\Delta\Sigma$ ADC [28], [29] embed the NS-SAR directly as the quantizer in a single modulator loop. Both approaches use a single quantizer, reducing second-stage hardware overhead. However, noise-coupling architectures typically require additional buffers and amplifiers for noise-coupling nodes, while NS-SAR-nested designs often suffer from reduced maximum stable amplitude and limited stability robustness due to their single-loop structure. In contrast, the LNC-SMASH places the NS-SAR in a dedicated second stage, improving stability at the cost of an additional first-stage quantizer.

III. Rail-to-Rail Low-Power Dynamic Amplifier

A. Design Constraints of the First Integrator's Amplifier

The first integrator of the circuit bears the most stringent thermal noise constraints since the input-referred noise of subsequent stages is suppressed by the integrator gain. This requires the use of large sampling capacitors to limit kT/C thermal noise, which in turn imposes high capacitive drive demands on the amplifier. For the LNC-SMASH, this challenge is further exacerbated by exploiting the high-order noise shaping to reduce the OSR and thereby achieve a more favorable bandwidth–SNDR trade-off for a given power budget. However, a reduced OSR requires even larger sampling capacitors, as the OSR thermal noise attenuation effect is lesser. In addition, the amplifier must satisfy stringent settling-time and open-loop gain requirements to ensure proper noise shaping and avoid SQNR degradation.

Although it is possible to design a conventional amplifier to fulfill these requirements, the associated static power consumption becomes prohibitively large, often exceeding that of the entire ADC. Numerous techniques have therefore been proposed over the years to improve amplifier power efficiency. Dynamic amplifiers (DA) [30], [31] modulate the bias current to reduce static power, while input-dependent biasing [32], [33] enhances slewing for large signals at the cost of extra current branches and added input capacitance. Slew-enhancement techniques inject current directly at the output [34], [35], but similarly increase complexity. Two-step or two-phase settling approaches [36]–[38] dynamically reconfigure the amplifier during slewing, either by temporarily interrupting the feedback loop [37] or switching resistive elements to modulate bandwidth [36], [38].

Among recent state-of-the-art solutions, DA have attracted attention due to the high FOM achieved in several implementations [7], [39]–[41]. Charge-steering DA have been proposed [25], [42], [43], but their variable output common-mode voltage and high PVT sensitivity necessitate careful calibration. Floating-inverter amplifiers (FIA) [7], [39], [44] address these issues using floating reservoir capacitors, but are limited in output swing and drive strength. In the LNC-SMASH case, the capacitor requirements of the first integrator are further exacerbated by the simultaneous needs for high SNDR and low OSR, rendering the necessary reservoir capacitor impractically large in the order of tens of picofarads.

B. Circuit Overview

To overcome these limitations and achieve a more favorable trade-off between static power consumption, capacitive drive strength, and silicon footprint, we propose a novel rail-to-rail amplifier that combines dynamic and static operation. The design, based on [45], is illustrated in Fig. 4 along with simplified waveforms. The class-AB output stage provides both high capacitive drive capability and rail-to-rail output swing. Dynamic operation is enabled by a variable current source that modulates the bias current according to the operating phase of the amplifier.

Since the amplifier is embedded in a switched-capacitor integrator, it operates in two phases: ϕ_1 the sampling phase

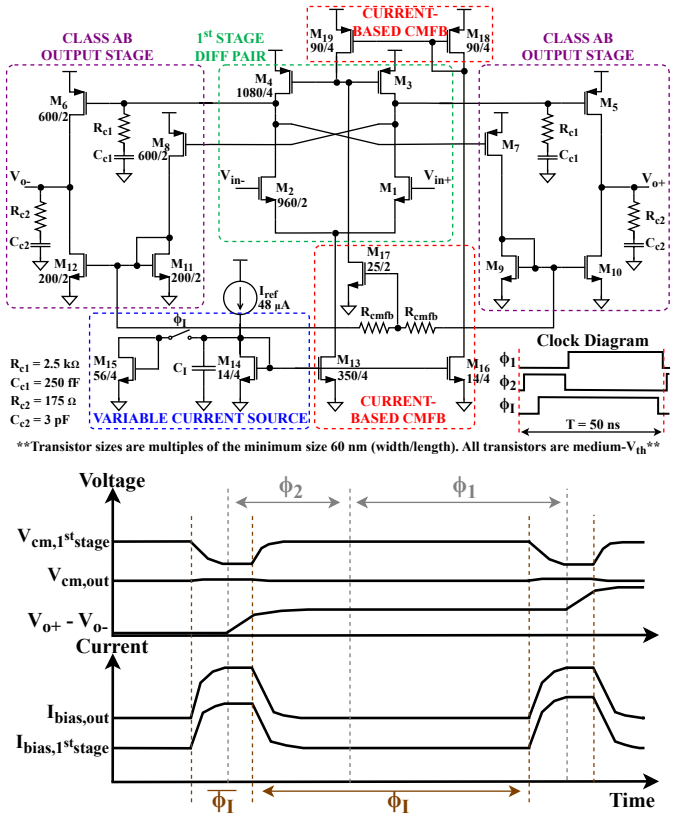

Fig. 4. Schematic of the proposed rail-to-rail dynamic amplifier with its simplified waveforms. Transistor sizes are shown for one half of the differential circuit. The output CMFB circuit is omitted for clarity.

and ϕ_2 the charge transfer phase. ϕ_2 begins with a slewing interval, where large bias currents are required to rapidly transfer charge. As the output approaches its final value, the amplifier transitions to linear settling, where lower bias currents suffice. In a conventional static design, high bias currents are maintained throughout the entire operation, resulting in high power consumption. In contrast, the proposed hybrid biasing scheme boosts the bias current only at the beginning of ϕ_2 to minimize the slewing time and then reduces it during the linear settling interval, thus optimizing power efficiency. During the sampling phase ϕ_1, the bias current is kept low as the amplifier remains idle.

The variable bias current is generated using a switched-ratio current mirror, which alternates between high and low current levels. To smooth the transition and suppress sharp transients, a capacitor C_I is added so that the bias current gradually converges from one level to another. An additionnal clock, ϕ_I, is required to control the variable current source and toggle between high and low bias current. This clock is fixed and transitions at the end of the slewing phase of the amplifier, as shown in Fig. 4.

The proposed design differs from conventional DA and slew-enhancement techniques by directly modulating the amplifier bias via the variable current source. This allows for minimal deviation from a baseline class-AB architecture, minimizing hardware overhead, and avoiding parallel signal paths or auxiliary amplifiers that would load the input and reduce static power savings. The main drawback is the need

for an extra clock phase to control the current source. Although producing such an additional clock phase may be impractical in a standalone amplifier, this concern is irrelevant in the LNC-SMASH since a multi-phase clock generator is required in any case.

Simulations demonstrate a 36% reduction in power consumption compared to a statically biased counterpart, reducing the power from 1.41 mW to 892 μW while maintaining the same transient response time. Although the improvement in power efficiency is less dramatic than that of FIA-based designs, the proposed amplifier provides key advantages: rail-to-rail operation, strong capacitive drive capability, and small footprint of capacitors.

C. Current-Based Common-Mode Feedback

In order to control the biasing currents of both stages using the same current source, a current-based common-mode feedback (CMFB) is proposed. Transistors M_{17} and M_{19} share the same current branch that sets the bias of the active load of the first-stage differential pair $M_{3,4}$, enforcing

$$I_{M_{17}} = I_{M_{19}}. \tag{2}$$

M_{17} is biased by the average of the output transistor bias voltage, such that:

$$I_{M_{17}} = \frac{1}{2} k_n \left(\frac{V_{ov_{M10}} + V_{ov_{M12}}}{2} \right)^2, \tag{3}$$

where square-law operation in saturation is assumed, k_n denotes the MOSFET transconductance parameter, and V_{ov} is the overdrive voltage. For small differential excursions between $V_{ov_{M10}}$ and $V_{ov_{M12}}$, this expression can be approximated as:

$$I_{M_{17}} = \frac{1}{k} \frac{I_{M_{10}} + I_{M_{12}}}{2}, \tag{4}$$

where k is the size ratio between $M_{10,12}$ and M_{17}, equal to 8 in this design. $(I_{M_{10}} + I_{M_{12}})/2$ is the average output bias current $I_{out_{avg}}$. The current $I_{M_{19}}$ is a direct copy of the variable input current source. Accordingly, from (2), the bias point of $M_{3,4}$ is set to satisfy:

$$I_{out_{avg}} = k \cdot l \cdot I_{ref}, \tag{5}$$

where l is the current-mirror ratio between the variable current source and M_{16}, varying between $1/5$ and 1 depending on ϕ_I. Consequently, I_{ref} simultaneously controls the output and the first-stage bias currents through different scaling factors.

Moreover, using this technique, the accuracy of the output bias current becomes only dependent on device matching (M_{14-16} and $M_{9,11,17}$), exhibiting great robustness to process variation. Fig. 5 presents results from a Monte Carlo simulation of the output stage bias current with both process and mismatch variations of the foundry models. For a nominal design target of about 90 μA, the current-based CMFB achieves a standard deviation of 5.5 μA, with the vast majority of samples falling between 80 and 100 μA. All simulated design instances met the required settling-time specifications for the LNC-SMASH.

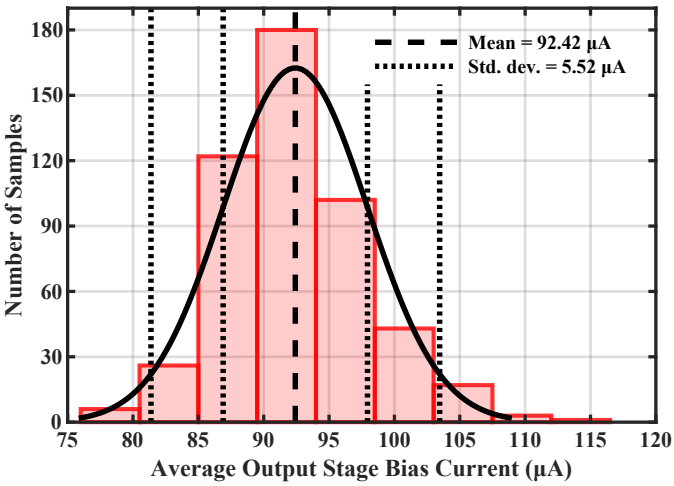

Fig. 5. Schematic-level Monte Carlo simulation with 500 runs showing the average output stage bias current using the proposed current-based CMFB technique.

D. Frequency Response

Fig. 6 shows the amplifier frequency response obtained from periodic steady-state analysis, which captures the effect of the variable bias current. Due to the large 12 pF sampling capacitor acting as a load, the response is dominated by the output pole. Rather than using Miller compensation and push this pole to high frequency, RC compensation networks are employed to introduce zeros and improve phase margin, enabling a more power-efficient design.

Each amplifier stage is therefore loaded by an RC network and a capacitive load C_L. Neglecting higher-frequency poles, the small-signal transfer function of both stages can be approximated as:

$$H(s) = \frac{g_m R_o (R_c C_c s + 1)}{R_c R_o C_c C_L s^2 + (R_c C_c + R_o C_c + R_c C_L) s + 1}, \tag{6}$$

where g_m is the stage transconductance and R_o the output resistance. The dominant output pole is approximately:

$$f_{p1} = \frac{1}{2\pi R_o C_L}, \tag{7}$$

while the compensating zero introduced by the RC network is located at:

$$f_z = \frac{1}{2\pi R_c C_c}. \tag{8}$$

For both the main amplifier and CMFB loops, the zero is placed slightly below the unity-gain bandwidth to provide positive phase boost at crossover, ensuring adequate phase margin. Although this approach is generally less robust than Miller compensation, simulations across process corners presented in Table I show great performance stability. Interestingly, the slow–slow corner exhibits the highest UGB due to the compensating zero shifting to lower frequency. As expected, the 3 dB bandwidth remains lowest in this corner, being set by the dominant output pole.

The amplifier noise is dominated by the input differential pair and can therefore be approximated by this contribution alone for noise analysis, as discussed in [46]. Periodic

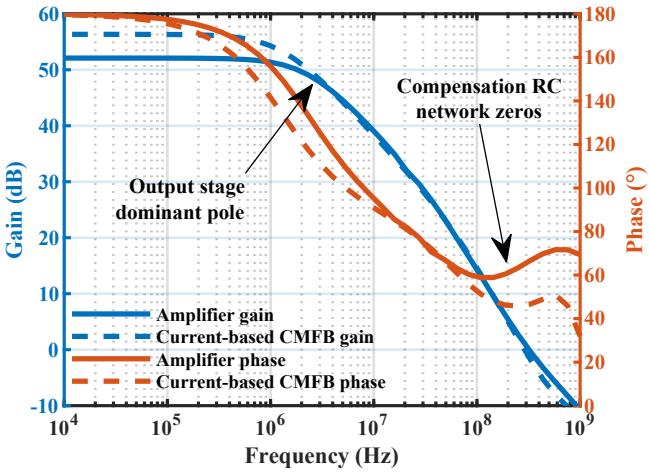

Fig. 6. Schematic-level periodic steady-state simulation results for the frequency response of the proposed dynamic amplifier and the associated current-based CMFB loop.

TABLE I
PERIODIC STEADY-STATE SIMULATION RESULTS OF THE PROPOSED DYNAMIC AMPLIFIER FREQUENCY RESPONSE ACROSS PROCESS CORNERS

Process corner	TT	SS	SF	FS	FF
DC gain (dB)	52.1	52.7	52.2	51.9	51.8
3 dB BW (MHz)	2.29	2.22	2.39	2.28	2.58
UGB (MHz)	322	427	339	316	337
Amplifier PM (°)	74	68	72	75	63
1st CMFB PM (°)	44	43	42	45	41
2nd CMFB PM (°)	61	56	55	70	76

steady-state noise simulations show an input-referred noise of 10.5 μV^2 without chopping. In the final ADC implementation, chopping is applied, reducing the input-referred noise to 1.7 μV^2.

IV. Passive Voltage Summing Circuit

A. Circuit overview

When the first-stage loop filter $F_1(z)$ is realized using a cascade-of-integrators-with-feedforward (CIFF) topology, a full-scale summing node is required prior to the first quantizer. Active summing amplifiers can provide this function but incur high power consumption due to the large signal swing. Passive switched-capacitor summation is therefore preferred for low-power operation, although conventional designs rely on additional sampling capacitors on the signal paths [44], [47].

In the proposed LNC-SMASH architecture, a more compact solution is implemented by reusing the capacitive DAC (CDAC) array of the SAR quantizer as the summing element. The concept is illustrated in Fig. 7. Instead of sampling the analog input on the entire capacitor array, dedicated switches in each DAC driver cell allow sampling of distinct analog voltages. The equivalent sampled voltage V_{samp} across the array is then given by the weighted sum of the sampled inputs' capacitance over that of the total array:

$$V_{samp} = \sum_{i=1}^{n} \frac{V_{in,ana(i)}}{2^i} + \frac{V_{in,ana(n+1)}}{2^n}, \tag{9}$$

where $V_{in,ana(i)}$ denotes the ith analog input sampled on the n-bit capacitor array, the MSB capacitor being at $i = 1$.

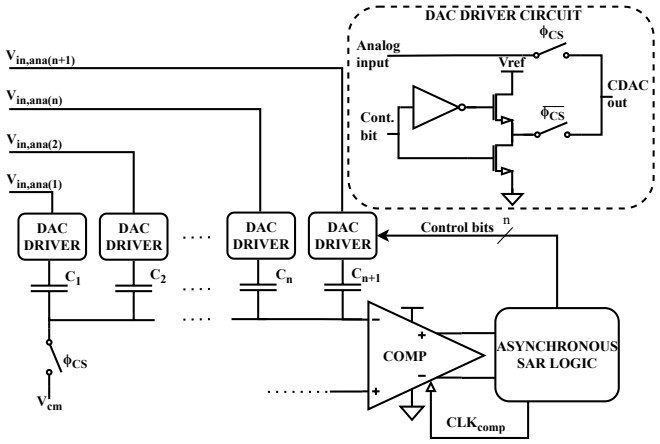

Fig. 7. Simplified schematic of the proposed passive summation scheme that reuses the SAR quantizer DAC capacitor array.

The summing coefficients are constrained by the binary-weighted nature of the array, which is required for correct SAR operation. However, different combinations of coefficients can be achieved by connecting multiple capacitors to the same analog input. For the LNC-SMASH implementation presented in the next section, a 3-bit SAR quantizer is employed, configured with one half-weight and two quarter-weight coefficients by tying the two smallest capacitors to the same analog input. To compensate for the signal attenuation introduced by the passive summer, the reference voltage of the SAR quantizer is scaled down by a factor of four. To ensure proper operation of the DAC driver logic at a lower reference voltage, the conventional inverter used to drive the CDAC is replaced by an all-NMOS pass-gate equivalent, as shown in the upper-right corner of Fig. 7.

While the technique is highly power- and area-efficient as it reuses the SAR capacitor array, it is inherently limited to binary-weighted combinations for implementing the NTF coefficients. This restricts design flexibility, especially in higher-order modulators, where achieving or tuning noise shaping for stability may not be possible. Increasing the number of bits expands the available coefficients but ties bit resolution to decisions pertaining to gain, thus again reducing design flexibility. Moreover, higher bit counts require a lower quantizer reference voltage to restore gain, increasing noise sensitivity. Therefore, the proposed approach represents a trade-off between power and area efficiency and design flexibility. The LNC-SMASH represents an ideal case where the desired second-order coefficients are readily available, enabling reduced power and area with limited drawbacks, although these benefits may not translate to other designs.

V. LNC-SMASH ΔΣ ADC Design

A. Design Overview

The ADC prototype based on the proposed LNC-SMASH architecture was designed in a 65 nm 1P9M CMOS process with a 1 V supply. The high-level block diagram of the ADC is shown in Fig. 8. The design targets demanding data acquisition applications that require an SNDR of about 90 dB and a bandwidth of 500 kHz under strict power constraints. The

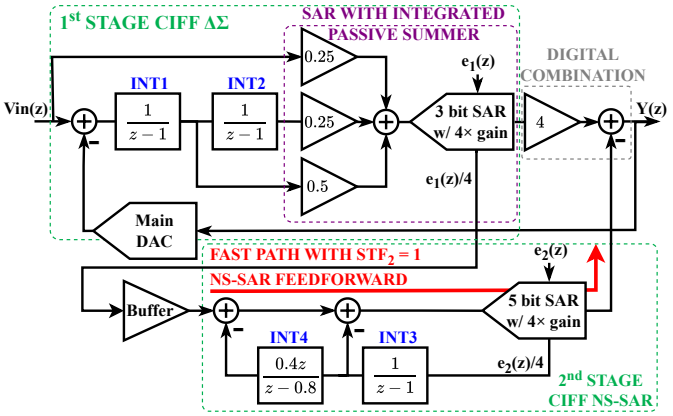

Fig. 8. Block diagram of the implementation of the LNC-SMASH ADC.

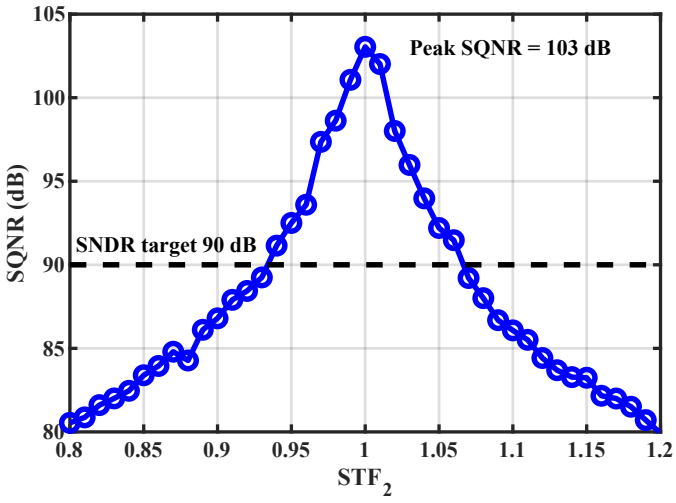

Fig. 9. System-level simulation of the SQNR sensitivity to STF_2.

first stage employs a second-order CIFF DT $\Delta\Sigma$ modulator incorporating the passive summation scheme described in Section IV. This topology offers low distortion and relaxed amplifier requirements due to reduced signal swing. The SAR quantizer error is sent to the NS-SAR second stage, also configured as a second-order CIFF. Together, the two stages achieve fourth-order noise shaping, enabling a low OSR of 20 and an efficient trade-off among power, SNDR, and bandwidth. To accommodate the fourfold reduction in the SAR error signal, the NS-SAR reference is also scaled by a factor of four. The final stage combination is handled in the digital domain, where appropriate scaling and subtraction complete the LNC-SMASH operation.

To maximize power efficiency, the design is thermal-noise-limited to an SNR of 90 dB. Assuming an ideal NTF of $(1-z^{-1})^4$, the resulting SQNR is significantly higher, reaching 109 dB. Consequently, the fourth integrator in the NS-SAR stage is simplified to a passive integrator to reduce area and power consumption, with negligible impact on the overall SNR. This modification lowers the ideal SQNR to 103 dB. The resulting signal and noise transfer functions of the final implementation shown in Fig. 8 are:

$$STF_1(z) = STF_2(z) = 1, \tag{10}$$

$$NTF_1(z) = (1 - z^{-1})^2, \tag{11}$$

$$NTF_2(z) = (1 - z^{-1})\frac{1 - 0.8z^{-1}}{1 - 0.4z^{-1}}. \tag{12}$$

B. First Stage Noise Leakage and Interstage Buffer

Extraction of the error signal from the first-stage SAR quantizer requires a unity-gain buffer amplifier to minimize noise leakage and ensure proper noise cancellation, as expressed in Eq. (1). Any deviation from unity gain directly affects STF_2, leading to incomplete cancellation of the first-stage error. The residual error is attenuated and shaped by NTF_1:

$$Y_{e_1}(z) = \alpha NTF_1 e_1(z), \tag{13}$$

where $Y_{e_1}(z)$ is the output contribution of the first-stage error and α represents the deviation from the ideal STF_2. While this error may arise from gain inaccuracies in the buffer or from non-ideal attenuation and scaling in the NS-SAR stage, simulation results indicate minimal deviation from unity gain within the NS-SAR itself, suggesting that buffer gain error is the dominant contributor.

To assess when first-stage quantization noise leakage becomes significant, the in-band noise of each stage is evaluated by assuming a white quantization noise source and integrating over the signal band [46]:

$$IBN_1 = \frac{{\Delta_1}^2}{12\pi}\int_0^{\frac{\pi}{OSR}} |\alpha NTF_1(e^{j\omega})|^2 d\omega. \tag{14}$$

Here, IBN_1 denotes the in-band noise due to the first-stage quantization error and Δ_1 is the corresponding quantizer step size. Applying the same approach to the second stage and approximating both NTF as ω^2 to enable closed-form integration [46] yields

$$IBN_1 = \frac{\alpha^2 {\Delta_1}^2 \pi^4}{60 \cdot OSR^5}, \tag{15}$$

$$IBN_2 = \frac{{\Delta_2}^2 \pi^8}{108 \cdot OSR^9}. \tag{16}$$

Assuming near-perfect cancellation such that $IBN_1 \ll IBN_2$, the resulting constraint on the gain error α of STF_2 is

$$\alpha^2 \ll \frac{5{\Delta_2}^2 \pi^4}{9{\Delta_1}^2 OSR^4}. \tag{17}$$

Equating both noise contributions for a -6 dB SQNR penalty yields a required STF_2 gain accuracy of 0.5% as per Eq. (17). The ω^2 approximation of the NTF is conservative, as the less aggressive implemented NTF_2, provides weaker noise shaping and increases the second-stage noise contribution. A numerical evaluation of the integral using the exact NTF from Eq. (11) and Eq. (12) results in an allowable gain error of 1.3%. Simulations shown in Fig. 9 confirm the trend: as STF_2 deviates from unity, the SQNR degrades, with a -6 dB penalty occurring at approximately a 3% gain error. The small discrepancy with the theoretical estimation is attributed to simplifying assumptions such as white noise spectrum and system linearization.

For a targeted SNDR of 90 dB, Fig. 9 shows that the allowable STF_2 gain error is below 6%. However, since the

design is limited by thermal noise, margin is required to prevent quantization noise from degrading accuracy. Maintaining SQNR above 97 dB, so as to limit quantization noise contribution below 20% corresponds to a tolerable gain error of 3%. Including an additional 2% margin for other error sources requires a minimum buffer open-loop gain of 40 dB, which is readily achievable. As the buffer operates in a unity-feedback configuration, no matching requirements are imposed on the feedback network. The buffer must also settle within the NS-SAR sampling interval of 7 ns while driving the NS-SAR capacitor array totaling 800 fF.

As a final remark, replacing the unity-gain buffer with a gain stage of factor ISG could, in principle, improve SQNR by $20\log ISG$ [20], [48]. However, this is impractical for the LNC-SMASH architecture. Introducing gain requires a feedback network subject to process mismatch, reducing the already tight STF_2 gain error margin of 3%. Moreover, maintaining a unity transfer function would require a digital division by ISG after the NS-SAR stage, increasing output word length and DAC resolution. Consequently, a unity-gain interstage buffer is retained in the proposed implementation.

C. Circuit Overview

Fig. 10 presents the complete circuit implementation together with the clock diagram. All circuit blocks, including the clock phase generator and digital combination logic, are implemented at the transistor level. Only the foreground calibration is performed off-chip. The first integrator, which faces the most stringent noise requirements, employs the proposed rail-to-rail dynamic amplifier introduced earlier. To mitigate flicker noise, chopping is applied at the amplifier inputs and outputs, while bootstrap sampling switches [49] are used to suppress harmonic distortion. The second integrator adopts a recycling folded cascode (RFC) amplifier [50], selected for its robustness and superior power efficiency compared to a conventional folded cascode. The amplifier simulation results demonstrate a DC gain of 50 dB and a UGB of 320 MHz with a phase margin of 52°.

The buffers employ class-AB Monticelli op-amps [51], [52], which deliver high output drive capability while preserving relatively high gain. The buffer's schematic-level simulation yields specifications of 49 dB DC gain, 350 MHz UGB, and 55° phase margin.

The CIFF NS-SAR leverages a hybrid active/passive loop filter, combining an FIA [39] with a passive switched-capacitor integrator that provides 2× gain [6]. In addition, a capacitor stacking technique [53] is adopted to sum the outputs of the NS-SAR loop filter efficiently, replacing the conventional multi-input comparator and avoiding its associated power overhead. The FIA design reaches specifications of 50 dB DC gain, 340 MHz UGB and 52° phase margin.

D. Timing Analysis

Fig. 11 presents the timing diagram of the proposed LNC-SMASH ADC. The time critical path is highlighted in red. As shown, the NS-SAR sampling and quantization operations must occur sequentially with the first-stage operation. To accommodate this timing constraint, the NS-SAR operation is designed to be a fast path, with a total duration of 20 ns, consuming slightly more than one third of the available timing budget. This constraint makes the LNC-SMASH architecture more suitable for moderate bandwidth applications, as the

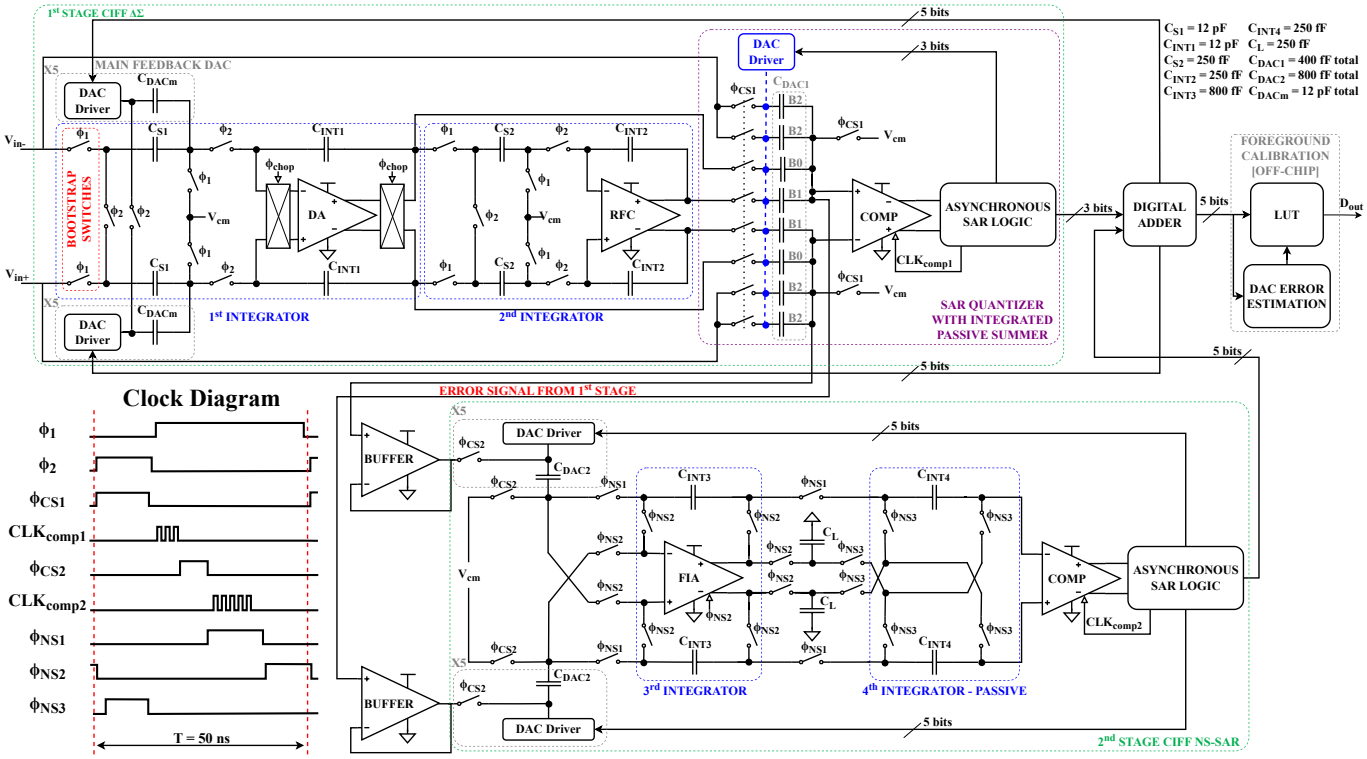

Fig. 10. Simplified schematic of the proposed LNC-SMASH ΔΣ ADC with clock diagram.

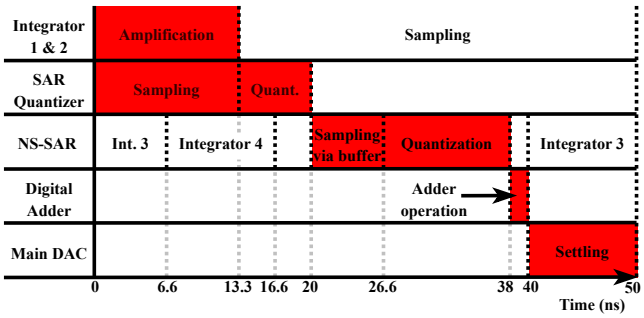

Fig. 11. Timing diagram for one period of the proposed ADC. The main time critical path is highlighted in red.

two stages operating in series ultimately limit the maximum achievable sampling speed. The NS-SAR loop filter, however, lies outside the critical path, which significantly relaxes its timing constraints.

A single 300 MHz input clock is required. All necessary clock phases are generated on chip using a divide-by-15 circuit, providing a timing resolution of 3.3 ns for the different clock phases over the 50 ns clock period.

E. Calibration Technique

The overall circuit architecture confines matching requirements solely to the main 5-bit feedback DAC, implemented as a binary capacitor array. Since DAC element mismatch errors are not shaped by loop filters, precise matching beyond the intrinsic foundry limits is required. To address this, a foreground calibration scheme is employed, executed at startup and/or periodically during operation, to digitally correct these errors. This work adopts the out-of-band tone method [54] to generate the lookup table used for DAC calibration.

Dynamic element matching (DEM) was not adopted as a replacement for calibration. Its effectiveness degrades at low OSR, and system-level simulations conducted in [20] showed that first-order DEM with the proposed LNC-SMASH low OSR and 5-bit quantizer is insufficient to recover 90 dB SNDR in the presence of mismatch. While higher-order DEM could improve performance, it would need to operate in series with the second-stage fast path, tightening timing constraints and increasing complexity. Consequently, an offline calibration strategy was preferred.

High-level simulations demonstrate that the ADC's accuracy is effectively restored to over 90 dB SNDR after calibration. As illustrated in Fig. 12, a 200-sample Monte Carlo analysis was performed, applying normally distributed random mismatches with a standard deviation of 2% to the DAC model to emulate a severe mismatch scenario. The results confirm that all calibrated cases exceed the 90 dB SNDR target.

Based on the simulation results including process-induced random variations presented in Fig. 17(a) of the next section, the foreground calibration achieves an average offset error of 185 μW (worst case: 490 μW) and an average gain error of 0.25% (worst case: 0.73%). The calibration uses 10k samples, corresponding to a latency of 500 μs.

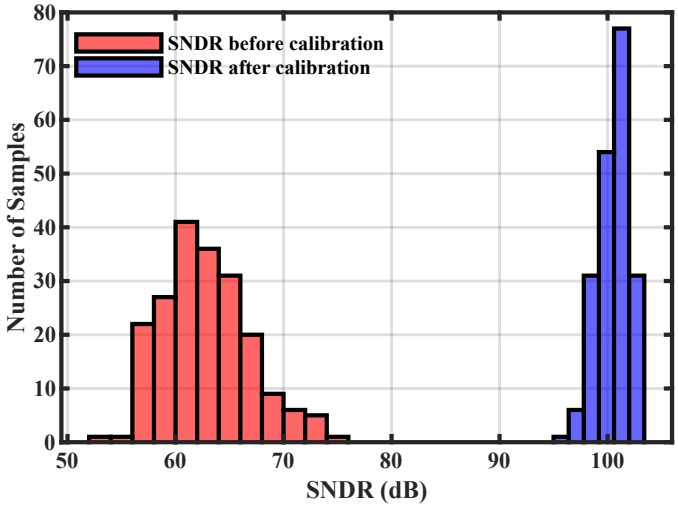

Fig. 12. System-level Monte Carlo simulation with 200 runs showing the SNDR of the proposed ADC under 2% standard deviation of DAC capacitor mismatch, before and after calibration.

F. Simulation Results

To ensure accurate SNR and SNDR estimation, all simulations include transient noise from foundry models. The simulated power spectral density (PSD) of the LNC-SMASH ADC is shown in Fig. 13(a). The results demonstrate an SNR of 91.9 dB, an SNDR of 89.1 dB, and a spurious-free dynamic range (SFDR) of 94.5 dB, highlighting the high precision achieved by the fourth-order modulator. The peak SFDR of 95.6 dB occurs at -6 dBFS input. Residual harmonics, primarily third- and fifth-order, account for the 2.8 dB gap between peak SNR and SNDR and limits the achievable SFDR. This distortion appears after replacing the ideal clock with its circuit-level implementation and is attributed to input-dependent leakage in the NS-SAR loop filter, likely from slower clock edges and extended non-overlapping phases. While further clock circuit optimization could reduce this effect, the small degradation was deemed acceptable for prototype validation.

Fig. 13(b) shows the PSD of each stage separately. Owing to its small sampling capacitors, the second stage exhibits a relatively high noise floor when considered in isolation. However, this contribution is effectively suppressed in the complete system by the gain of the first stage. The first stage alone achieves an SNR of 65.5 dB, indicating that the additional noise shaping provided by the second stage yields a 26.4 dB improvement to reach the overall SNR of 91.9 dB in the full LNC-SMASH implementation.

Fig. 14 illustrates SNR and SNDR as a function of input amplitude. Distortion remains low across the entire operating range, as the SNDR curve closely follows the SNR up to the maximum input amplitude of –2 dBFS. The resulting dynamic range is 95.1 dB.

The power breakdown of the simulated LNC-SMASH circuit is shown in Fig. 15. Although the dynamic amplifier technique applied in the first integrator reduces its power consumption by 36%, this block still accounts for slightly more than half of the total power budget of the ADC. In contrast, the second-stage NS-SAR is highly efficient, consuming only

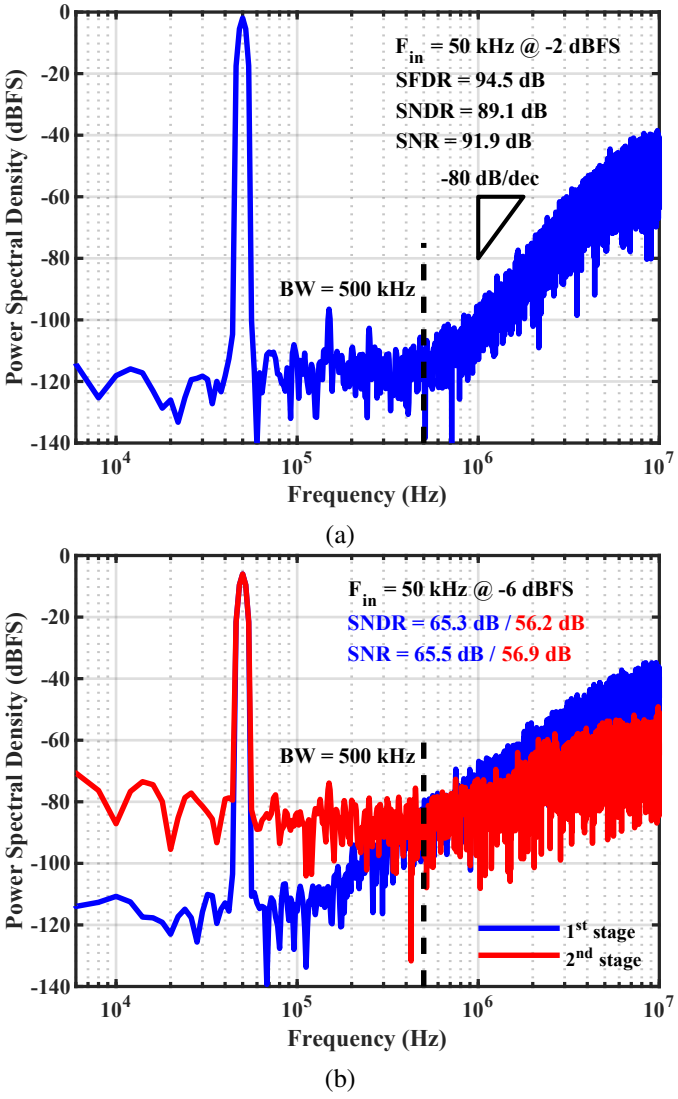

Fig. 13. Schematic-level simulated power spectral density of (a) the proposed ADC and (b) each of its stages separately.

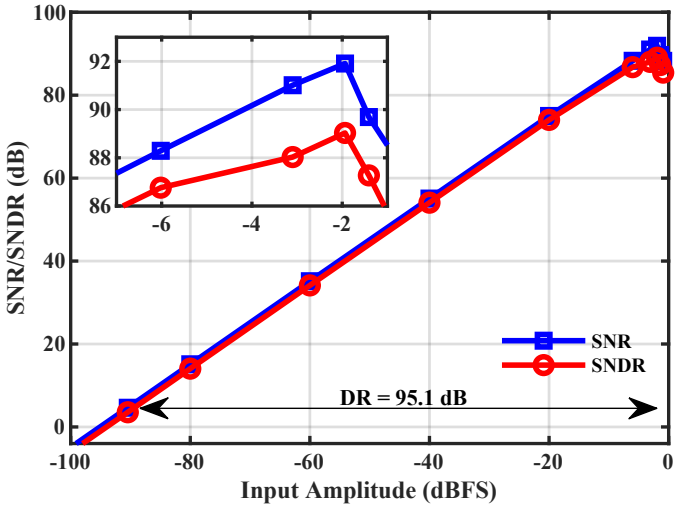

Fig. 14. Schematic-level simulated SNR and SNDR for varying input amplitude at 50 kHz.

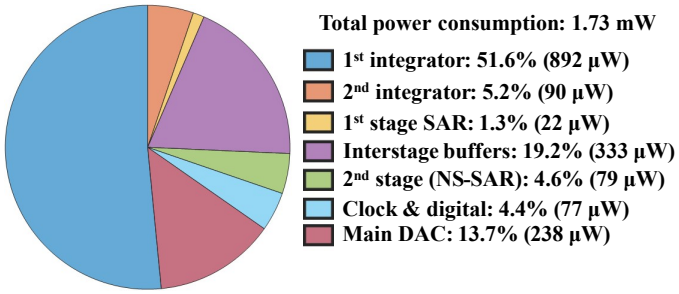

Fig. 15. Breakdown of the schematic-level simulated power consumption for subcircuits of the proposed ADC.

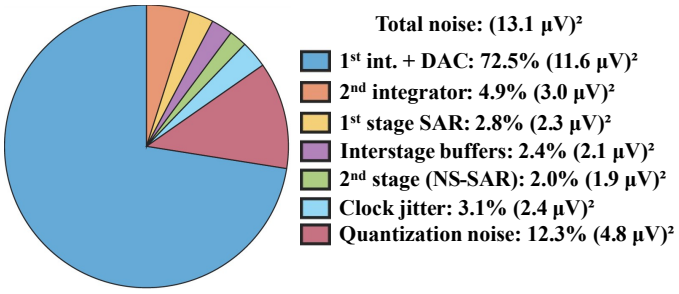

Fig. 16. Breakdown of the schematic-level simulated noise contribution for subcircuits and quantization noise of the proposed ADC.

79 μW while providing both noise shaping and cancellation of the first-stage quantization error. Even when including the interstage buffers, the additional circuitry required for the second stage represents less than one quarter of the overall power budget. The total ADC power consumption is 1.73 mW.

The noise breakdown is shown in Fig. 16, based on transient noise simulations at a -6 dBFS input. As expected, the first integrator circuit, which includes the feedback DAC and input sampling, dominates the noise budget, contributing 72.5%. Quantization noise accounts for 12.3%, while other subcircuits contribute only minor amounts.

To assess the robustness of the LNC-SMASH architecture, simulations were performed across process, temperature, and supply voltage (PVT) variations, as shown in Fig. 17. The y-axis reports the degradation of SNR and SNDR in dB, where negative values indicate performance degradation relative to a nominal simulation without PVT variations. Since the plotted values represent degradation rather than absolute performance, the SNDR curve may occasionally appear higher than the SNR curve. This simply indicates that the SNDR experienced slightly less degradation than the SNR, while the absolute SNR remains higher than the SNDR in all cases.

The sensitivity of SNR and SNDR to process variation is shown in Fig. 17(a). Due to the prohibitive simulation time, only a limited number of runs were performed, including both mismatch and random process variations from the foundry models. In sample 6, a worst-case mismatch was introduced by manually reducing one feedback DAC capacitor to 350 fF from its nominal 375 fF. As can be seen, the calibration is highly effective, as performance almost recovers to full accuracy. After calibration, the degradation of the SNR and SNDR remains within around 3 dB for all tested runs, demonstrating strong robustness despite the limited sample size.

To further evaluate process robustness without excessive

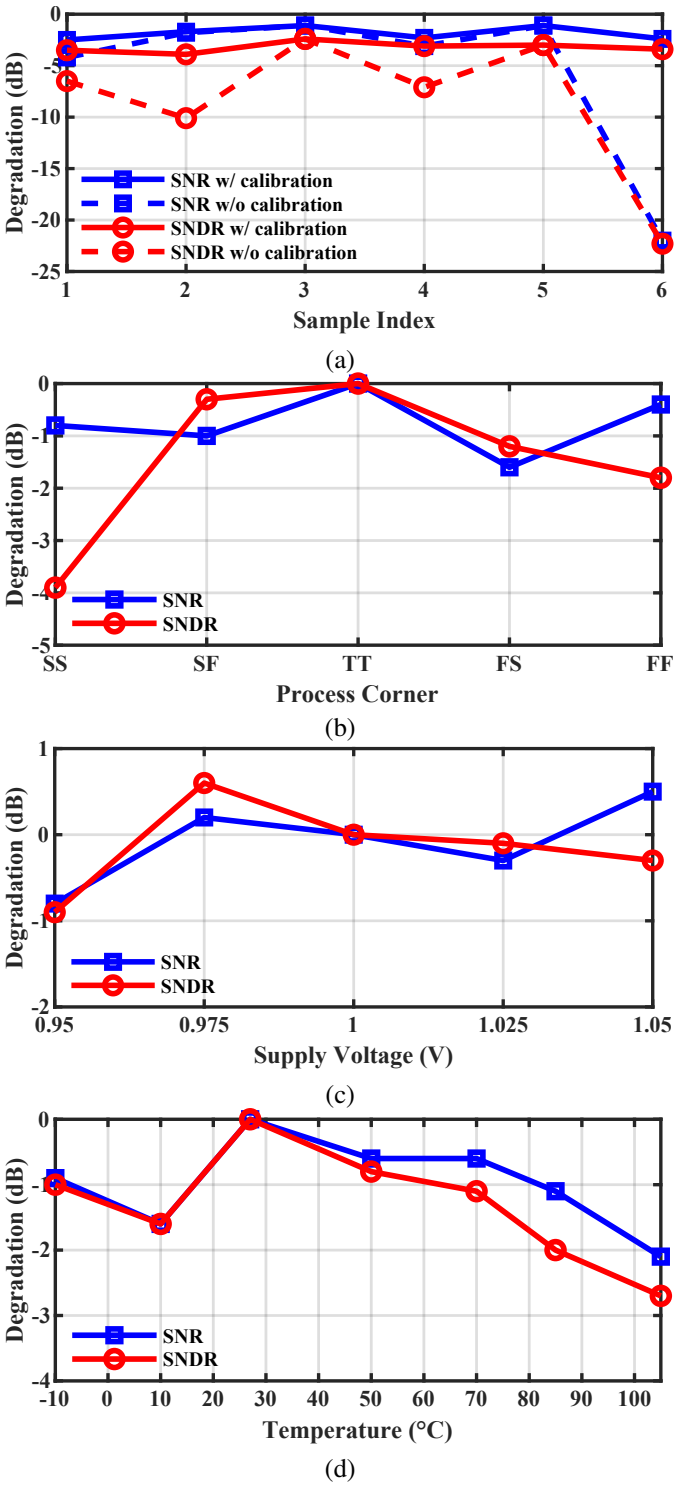

Fig. 17. Schematic-level simulated SNR and SNDR sensitivity to (a) process random, (b) process corner, (c) voltage and (d) temperature variations.

simulation time, process-corner simulations were performed, as shown in Fig. 17(b). These simulations include only deterministic process variations, without random mismatch, and therefore do not require calibration. All corners exhibit performance degradation below 2 dB, with the exception of the SNDR at the SS corner. Overall, the design shows satisfactory robustness to process variations.

The impact of supply and temperature variations is illustrated in Fig. 17(c) and Fig. 17(d), respectively. A ±5% supply voltage variation was considered, which is sufficiently wide given that the ADC is intended to be powered by a low-noise precision linear regulator with minimal deviation over the nominal 1 V supply. Under these conditions, the performance degradation remains below 1 dB. Temperature simulations were conducted over a range of -10 °C to 105 °C to cover the majority of expected operating conditions, including hot cases where the circuit operates alongside other heat-generating blocks on the same die. The resulting performance variation remains below 3 dB. Overall, the ADC maintains stable performance across PVT variations, confirming the robustness of the proposed architecture.

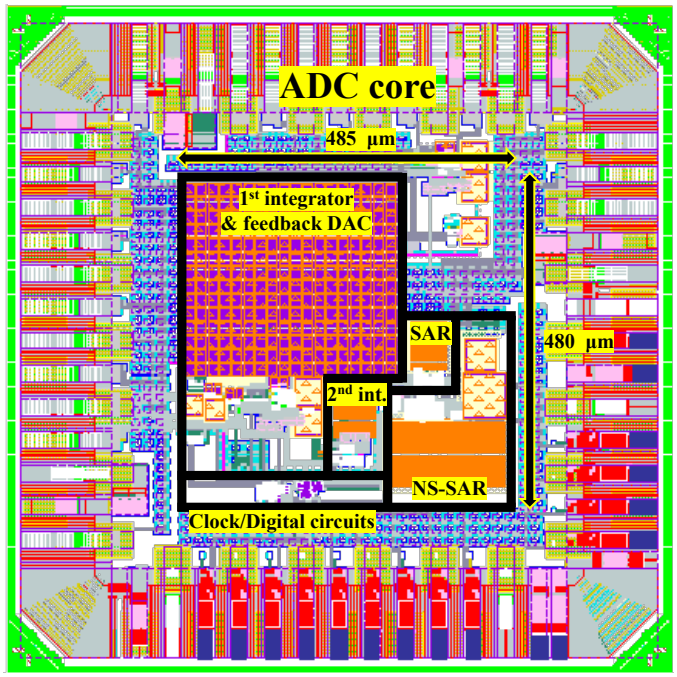

Fig. 18. Layout of the proposed LNC-SMASH ΔΣ ADC designed in 65 nm CMOS technology.

G. Layout and Post-Layout Simulations

Fig. 18 shows the layout of the designed LNC-SMASH ΔΣ ADC. The ADC core occupies a 485 μm × 480 μm rectangle. Taking into account the notch in the upper right corner, the active core area is 0.198 mm^2. The dominant contributor is the large 12 pF sampling capacitor, required to limit thermal noise and meet the target 90 dB SNR, while the rest of the architecture remains compact and circuit-efficient. Although the overall layout is not fully symmetric to enable better compactness between functional blocks, all CDAC and switched-capacitor integrator capacitor arrays are implemented using common-centroid MiM capacitors.

Post-layout simulations with parasitic extraction were performed to evaluate performance degradation after fabrication. The resulting PSD is presented in Fig. 19, with the pre-layout simulation results superimposed for comparison. The post-layout results exhibit slightly increased distortion, notably higher fifth-harmonic content due to residual CDAC mismatch after calibration, along with increased high-frequency noise

near the lower end of the noise-shaping slope. This noise increase is attributed to parasitic attenuation reducing STF_2, which enhances first-stage noise leakage and quantization noise. Overall, the impact is limited, with only about a 4 dB degradation in SNR and SNDR.

H. Comparison with State-of-the-Art Designs

Table II summarizes the performance of the simulated LNC-SMASH $\Delta\Sigma$ ADC and compares it with recent state-of-the-art designs. Since the proposed ADC is currently evaluated only through simulations, its results may be somewhat advantaged in comparison to physical implementations. As discussed in the PVT and parasitic-extracted simulations, real-world operation could introduce slight performance degradation. Nevertheless, even accounting for such effects, the LNC-SMASH remains highly competitive.

The FOM_{Sc} and FOM_{Wa} account for SNDR, power consumption, and bandwidth to evaluate ADC performance. The FOM_{Sc} places greater emphasis on SNDR, whereas FOM_{Wa} weighs power efficiency more heavily [4]. A higher FOM_{Sc} and a lower FOM_{Wa} both indicate superior performance. Under these metrics, the LNC-SMASH outperforms previously reported SMASH architectures while occupying a comparatively small silicon area. Furthermore, its FOM are comparable to those of many other state-of-the-art designs [27], [56], [57].

When compared with the state-of-the-art CT $\Delta\Sigma$ ADC reported in [56], the LNC-SMASH achieves an order-of-magnitude lower power consumption while doubling the bandwidth, highlighting its strong power efficiency. However, the design in [56] attains an exceptionally high resolution exceeding 100 dB SNDR and demonstrates a resolution-bandwidth combination that surpasses the proposed design.

As expected, conventional NS-SAR converters remain unmatched in terms of area and power efficiency. However, none of the recent NS-SAR designs achieve an SNDR above 89 dB with a bandwidth of 500 kHz or greater. Fig. 20 further illustrates this point by compiling designs from the past five

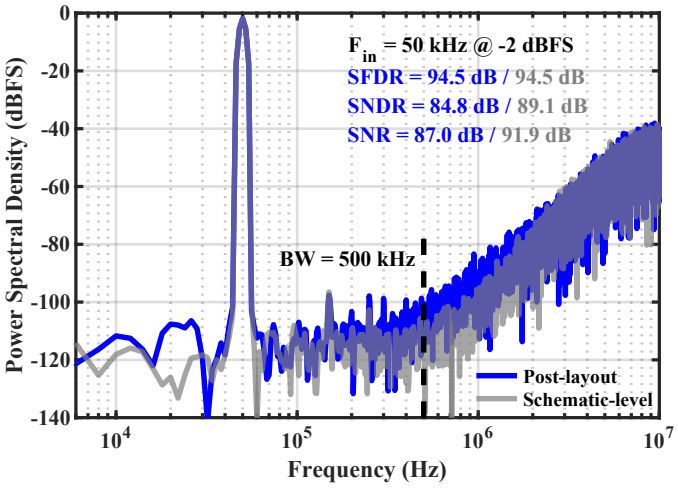

Fig. 19. Post-layout simulated power spectral density of the proposed ADC.

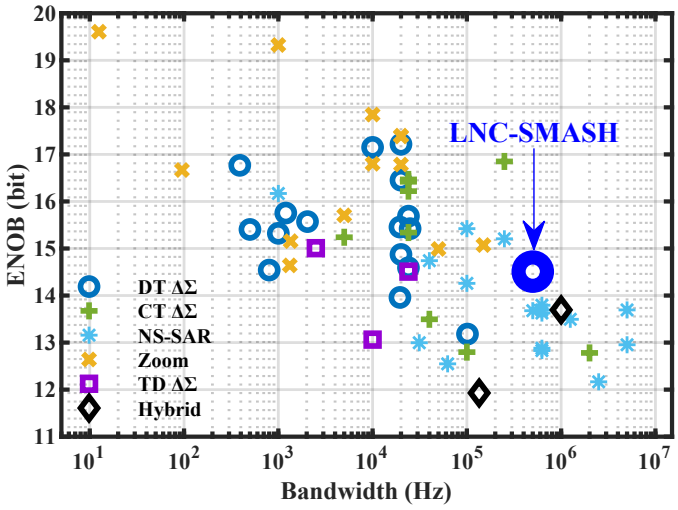

Fig. 20. Scatter plot of bandwidth and ENOB specifications for 60 recent oversampling ADC designs with FOM_{Sc} above 172 dB. The proposed LNC-SMASH design point is highlighted.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART $\Delta\Sigma$ ADC

	This work	[55]	[14]	[16]	[19]	[56]	[6]	[10]	[9]	[57]	[27]
Architecture	**LNC-SMASH**	Noise-coupled DT $\Delta\Sigma$	SMASH	SMASH	SMASH	CT $\Delta\Sigma$	NS-SAR	NS-SAR	NS-SAR	Hybrid VCO+NS-SAR	Noise-coupled CT $\Delta\Sigma$
Meas./sim.	**Sim.**	Sim.	Meas.	Meas.	Meas.	Meas.	Meas.	Meas.	Meas.	Meas.	Meas.
Process	**65 nm**	65 nm	180 nm	65 nm	65 nm	180 nm	40 nm	65 nm	65 nm	28 nm	28 nm
Calibration	**yes**	no	no	no	no	no	yes	yes	yes	no	no
Area (mm^2)	**0.198**	–	1.92	0.34	0.15	1.1	0.094	0.075	0.04	0.024	0.17
Supply (V)	**1**	1.2	1.2	1.2	1.1/1.3	1.8	1.1	1.2/2	1.1	1.8/1.2/1	1.1
Power (μW)	**1730**	290	3200	20400	12500	17700	340	73.8	119	1620	380
F_s (MS/s)	**20**	25	20	500	500	48	5	5	10	100	12.8
OSR	**20**	25	16	12.5	16	96	10	5	8	50	32
BW (kHz)	**500**	500	625	20000	15625	250	250	500	625	1000	200
SNR (dB)	**91.9**	93.0	75.6	73.7	79.4	104.3	94	–	85.1	84.9	89.2
SNDR (dB)	**89.1**	89.5	74.6	72.9	74	103.2	93.3	84.1	84.8	84.2	89.0
SFDR (dB)	**95.6**	–	89.7	–	84.2	–	104.4	97	103	97.3	103.9
FOM_{Wa}	**74.2**	11.9	583.3	141.3	97.7	299.6	18.0	5.6	6.7	61.1	41.2
FOM_{Sc}	**173.7**	181.9	157.5	162.8	165.0	174.7	182.0	182.4	182.0	172.1	176.2

$FOM_{Wa} = Power/(2^{ENOB}F_s)$ $[fJ/conv.-step]$; $FOM_{Sc} = SNDR + 10log(BW/Power)$ $[dB]$.

years with FOM_{Sc} above 172 dB [4]. The figure highlights the stringent design space addressed by the LNC-SMASH as it is the only architecture delivering more than 14-bit ENOB at bandwidths in excess of several hundred kilohertz.

VI. Conclusion

In conclusion, this work presents a novel $\Delta\Sigma$ ADC architecture, the LNC-SMASH, which leverages the NS-SAR's feed-forward property to efficiently implement noise cancellation. A dynamic amplifier and a capacitive summation scheme that reuses the SAR quantizer capacitors are also introduced, providing favorable trade-offs between power consumption and capacitor area. Simulations demonstrate excellent performance relative to state-of-the-art oversampling ADC, particularly in meeting stringent specifications that combine high SNDR with moderate-to-high bandwidth and low power consumption, and which are likely to grow in relevance along the developing applications landscape.

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