

# A Lean Noise-Cancelling Sturdy MASH Delta-Sigma ADC with a Noise-Shaping SAR Stage

Antoine Verreault<sup>1</sup>, *Student Member, IEEE*, Paul-Vahé Cicek<sup>2</sup>, *Member, IEEE*,  
and Alexandre Robichaud<sup>1</sup>, *Member, IEEE*

<sup>1</sup> Department of Applied Sciences, Université du Québec à Chicoutimi (UQAC), Chicoutimi, Canada

<sup>2</sup> Department of Computer Sciences, Université du Québec à Montréal (UQAM), Montréal, Canada

**Abstract**—This paper introduces a lean noise-cancelling sturdy-MASH delta-sigma ADC, achieved through the implementation of a noise-shaping SAR second stage, the use of which instead of the usual delta-sigma stage, eliminates, by virtue of its inherent feedforward mechanism, the quantization noise of the first stage. Moreover, any mismatch-induced error of the noise-shaping SAR gets shaped by the first stage, circumventing the need for strict capacitor matching or calibration. The elimination of noise-cancelling and/or calibration circuitry, as well as the inclusion of the area-efficient noise-shaping SAR qualify this topology as lean. Simulations demonstrate a proof-of-concept design achieving 107.7 dB SQNR for an OSR of 14 over a 1 MHz bandwidth.

**Index Terms**—Analog-to-digital converter (ADC), noise-shaping SAR, delta-sigma modulator, multi-stage noise shaping (MASH), sturdy MASH (SMASH).

## I. INTRODUCTION

In this budding era of widespread implementation of Internet of Things (IoT) and wireless sensor networks (WSN), the demand for high precision, low-power analog-to-digital converters (ADC) has never been greater. Such applications prioritize high signal-to-noise ratio (SNR), power efficiency and cost effectiveness, while a relatively low bandwidth of up to 1 MHz is typically sufficient to meet the requirements [1].

Noise-shaping successive approximation (NS-SAR) [2] is a promising architecture to meet the needs of sensor networks. Incorporating a SAR quantizer within an error-feedback delta-sigma ( $\Delta\Sigma$ ) topology, the NS-SAR architecture is power-efficient, low cost and process scaling friendly [3]. However, to achieve high SNR, the signal-dependent error of the SAR's capacitive digital-to-analog converter (CDAC) must be limited, typically by means of foreground calibration [1, 3], increasing complexity and power consumption.

The  $\Delta\Sigma$  architecture has long been a candidate for high SNR applications, but it is vulnerable to process scaling as it struggles with the reduced transistor gains of recent technology nodes [4]. Another inconvenience of  $\Delta\Sigma$  ADC is the limited practical bandwidth due to high oversampling ratio (OSR). OSR can be reduced for higher order modulator noise-shaping, at the price of stability problems [5].

To overcome the respective limitations of the NS-SAR and  $\Delta\Sigma$  architectures, combinations of both structures have been proposed. Multi-stage noise-shaping (MASH) [6] structures combine two stages of  $\Delta\Sigma$  modulators to increase noise-shaping order, cancel the first stage error and alleviate stability problems [5]. However, tight matching between the analog and digital circuit blocks is required to combine the two stages,

which poses a challenge as PVT variations can introduce mismatch and degrade SNR due to noise leakage [5]. Several combinations of NS-SAR in MASH structures have been proposed, for example two NS-SAR in a conventional MASH [7] or a pipeline MASH structure [8].

To alleviate the mismatch sensitivity inherent to the MASH architecture, the sturdy MASH (SMASH) architecture was introduced, which relies on analog feedback rather than digital cancellation to combine the two stages, eliminating the need for precisely matched digital blocks [9]. However, in SMASH, the error of the first stage is no longer cancelled, but merely attenuated by the high order noise-shaping [5]. Noise-cancelling SMASH (NC-SMASH) has been proposed to eliminate the error of the first stage like in MASH, but delay matching or additional circuit blocks are then necessary [10, 11]. Either SMASH or NC-SMASH incorporating a NS-SAR stage has yet to be explored.

This work proposes a discrete-time (DT) lean NC-SMASH (LNC-SMASH)  $\Delta\Sigma$  ADC with a NS-SAR second stage. In this novel topology, the noise of the first stage is cancelled by a fast path provided by the inherent feedforward property of the NS-SAR second stage [3]. Since the first stage error is nullified, a quantizer with a low bit count can be used to minimize power consumption and size for that DT  $\Delta\Sigma$  stage. As for the remaining error originating within the NS-SAR second stage, it is shaped by the filters in both the first and second stages, ensuring a high SNR at low power consumption. In addition to these benefits, the proposed architecture improves overall robustness and relaxes design constraints by having signal-dependent errors of the second stage shaped by the DT  $\Delta\Sigma$  first stage. As a result, the potential of the proposed ADC is very promising for high precision, low-power applications.

This paper begins with a brief review of SMASH and a description of the proposed architecture in section II. Simulation results are discussed in section III, while section IV presents the conclusions of this work.

## II. SYSTEM OVERVIEW

### A. Limitations of the SMASH Architecture

Fig. 1a shows the block diagram of a classic SMASH  $\Delta\Sigma$  ADC. Unlike the MASH structure, this configuration eliminates the need for separate digital filters because signal combination occurs before filtering. This relaxes the op-amp gain requirements necessary to obtain proper matching

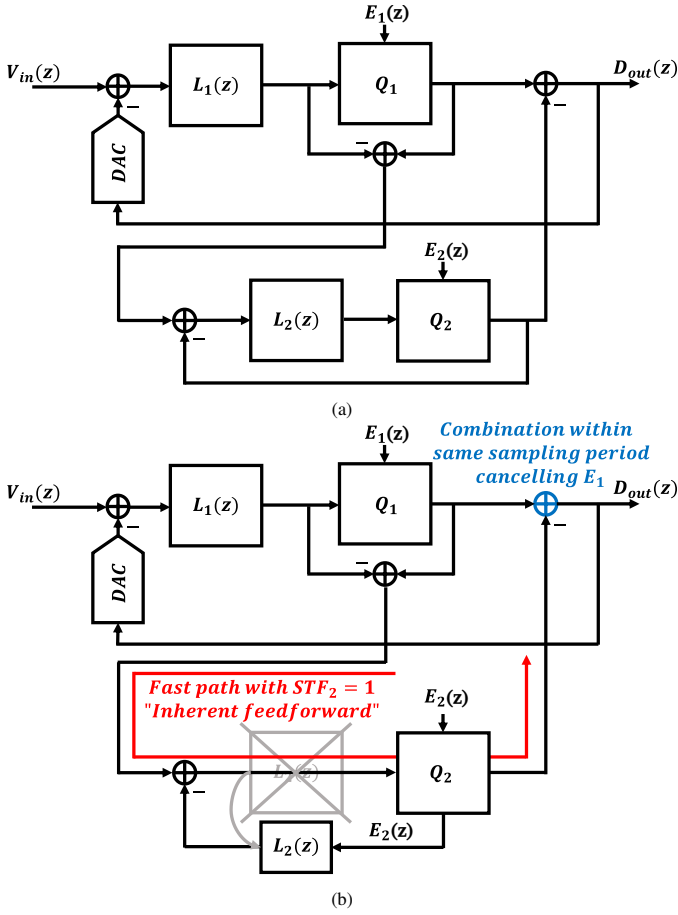


Fig. 1: Diagram of (a) the SMASH architecture and (b) the novel LNC-SMASH architecture.

between analog and digital sections [9]. The transfer function of the SMASH structure is:

$$D_{out}(z) = STF_1 V_{in}(z) - NTF_1 NTF_2 E_2(z) + NTF_1 (1 - STF_2) E_1(z), \quad (1)$$

with  $STF_n$  and  $NTF_n$  respectively the signal and noise transfer function of the  $n^{\text{th}}$  stage. Generally,  $STF_2$  is designed to be equal to  $1 - NTF_2$  so that the error of both stages is shaped by the same transfer function [5]. In that case, to achieve a given SNR, both stages must have the same bit count, tightening design constraints and increasing area.

The appealing option of instead setting  $STF_2 = 1$  to completely cancel the noise of the first stage would require a delay-free transfer function for the second stage, which is only archivable with an additional feedforward path and tighter timing constraints, increasing power consumption and area [5, 9]. The NC-SMASH in [11] introduces a delay, as well as a compensation DAC, to maintain stability, so that the term  $(1 - STF_2)$  in (1) transforms into  $(z^{-1} - STF_2)$ , resulting in an easier to implement signal transfer function of  $z^{-1}$  to cancel  $E_1$ , albeit at the expense of added circuitry.

### B. System-Level Implementation

The modifications proposed in the new LNC-SMASH architecture are presented in Fig. 1b. By using a NS-SAR in the second stage, a fast path is created between input and output of the second stage by virtue of the relocation of the loop filter

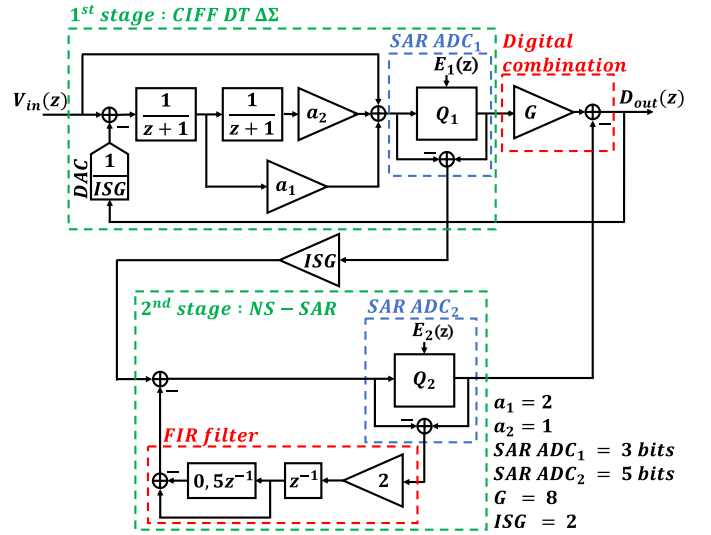


Fig. 2: Diagram of the proposed LNC-SMASH with NS-SAR stage.

onto the error feedback path. Achieving  $STF_2$  of 1 without added delay is now straightforward as there are no longer any integrators on the signal path. Provided that the quantizer is sufficiently fast to deliver its output within the same sampling period, combination will be able to occur before the next sample is captured. In [3], the NS-SAR topology is deemed “inherently feedforward” due to the signal path avoiding the loop filter. From (1), the unity  $STF_2$  of the NS-SAR allows for cancellation of the quantization noise of the first stage, such that:

$$D_{out}(z) = STF_1 V_{in}(z) - NTF_1 NTF_2 E_2(z). \quad (2)$$

This effect has the important benefit of relaxing the constraints on the bit count of the first stage quantizer, which results in a more favorable trade-off between power, area, and SNR.

Fig. 2 presents a detailed block diagram of the proposed system-level implementation. The first stage consists of a DT  $\Delta\Sigma$  structured as a cascade of integrators with feed forward (CIFF). DT implementation is selected for its robustness since loop coefficients depend on capacitor ratios instead of RC time constants [5]. CIFF is chosen for its low power and low distortion due to reduced amplitude swing in the integrators and only one DAC needed for feedback. The use of a SAR quantizer in this stage is optimal because it is able to directly generate the residue error for the second stage, eliminating the need for any additional adder or DAC component.

As for the second stage, NS-SAR is sensitive to non-linear errors on its SAR CDAC and FIR filter. These error sources introduce harmonic distortion in the signal and can be modeled as additive noise sources [3]. By having a DT  $\Delta\Sigma$  as the first stage, these errors will be shaped by  $NTF_1$ , mitigating their impact. As such, the matching and linearity requirements of the NS-SAR are relaxed so that calibration is no longer essential, further lowering the power and area needs of the already-efficient NS-SAR stage.

The combination of the two stages is performed by means of a digital adder so that the subtraction is error free and to remove the need for an additional feedback DAC. A gain  $G$  of 8 is added in series with the output of the first stage to bring the 3-bit  $SAR ADC_1$  to the same scale as the 5-bit

$SAR\ ADC_2$ . An interstage gain ( $ISG$ ) of 2 is also included to make use of the entire second stage quantizer range and improve signal-to-quantization-noise ratio (SQNR) [12]. The subsequent division by 2 is implemented in the feedback DAC, which contains 96 unit elements with halved weight.

The proposed topology is qualified as “lean” because it allows important reduction of the requisite circuit blocks in comparison to a standard NC-SMASH. The inherent feedforward of the NS-SAR stage provides noise cancelling without the cost of added circuitry, while relaxing the constraints on the first stage. Furthermore, the NS-SAR stage itself is highly area efficient as it doesn’t require calibration and the loop filter is simpler than in the  $\Delta\Sigma$  counterpart. Finally, the use of SAR quantizers in each stage allows the provision of the error signals without the need for additional DAC and summers.

The noise cancellation decreases the input levels processed by the quantizers and the loop filters, reducing the risk of saturation and making aggressive  $NTF$  achievable with a looser constraint on maximum input amplitude. All gain coefficients in the system are designed to yield  $(1 - z^{-1})^2$  for both  $NTF$ .

### C. Proof-of-Concept Design

A proof-of-concept design intended for a 65 nm node with 1.2 V supply was realized at system level to test the new architecture. The design aims for a target signal-to-noise-and-distortion ratio (SNDR) superior to 90 dB after fabrication, with a 15 dB margin. To determine the requisite OSR and quantizer number of bits, the following theoretical SQNR expression is used [5, 12]:

$$SQNR_{dB} = 10 \log \frac{6A^2(2L+1)OSR^{2L+1}ISG^2}{\pi^{2L}\Delta^2}, \quad (3)$$

with  $A$  the input amplitude,  $L$  the modulator noise-shaping order and  $\Delta$  the voltage interval between 2 quantizer levels in the second stage. It is determined that a 5-bit quantizer with an OSR of 14 yields a theoretical SQNR of 107.8 dB for an input of -3 dBFS, meeting design requirements. Expected bandwidth is 1 MHz for a 28 MS/s sampling rate.

## III. SIMULATION RESULTS

System-level simulations were conducted in MATLAB and Simulink as a first proof of concept for the new ADC architecture. Parts of the model and functions used for calculation were inspired by Schreier’s toolbox [5, 13].

### A. Simulation of Ideal Output SQNR

Fig. 3 presents the output power spectrum density (PSD) for -3 dBFS input at 100 kHz. It can be observed that the noise shaping slope is indeed -80 dB/dec confirming the 4<sup>th</sup> order modulator behaviour. Simulated SQNR is 107.7 dB which is very close to the theoretical calculation of 107.8 dB with (3).

Fig. 4 compares the output SQNR at varying OSR for the proposed LNC-SMASH compared to simulated scenarios based on 1) the 2-2 SMASH of [9] with a 3- and a 5-bit quantizers (same as this work), 2) that 2-2 SMASH again but with two 5-bit quantizers (to account for its first stage not benefiting from noise cancellation) and 3) the second-order NS-SAR of [14] with a 7-bit quantizer (overall capacitor footprint similar to this work). The proposed LNC-SMASH topology achieves the best noise-shaping throughout the evaluated OSR due to

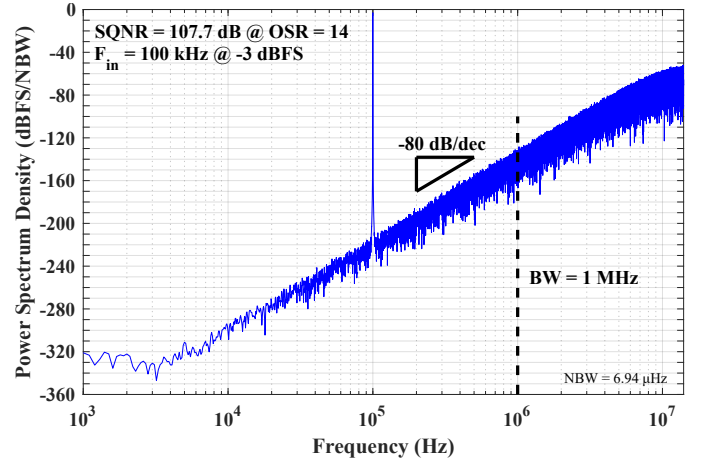


Fig. 3: Simulated output power spectrum density of the proposed ADC.

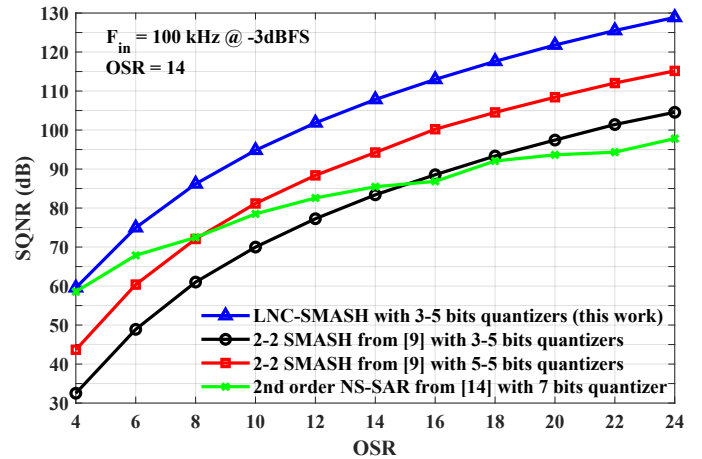


Fig. 4: Comparison of the SQNR for the LNC-SMASH of this work with a 2-2 SMASH and an NS-SAR with equivalent capacitor area.

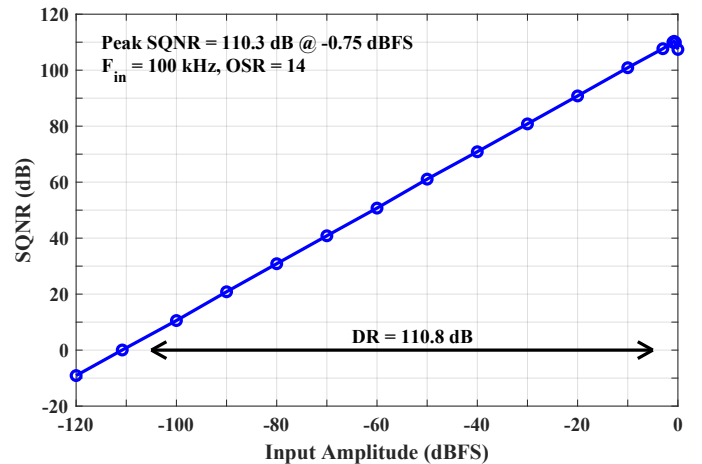


Fig. 5: Simulated SQNR with varying input amplitude.

its noise cancellation, high order noise shaping and efficient synergy of the two stages.

Fig. 5 shows the effect of varying input amplitude on SQNR. Peak SQNR of 110.3 dB is achieved for -0.75 dBFS. The dynamic range (DR) is 110.8 dB.

### B. Simulation of Mismatch Effect on SNDR

Assuming CDAC-based SAR quantizer and capacitive feedback DAC outputting in the switched capacitor integrator of

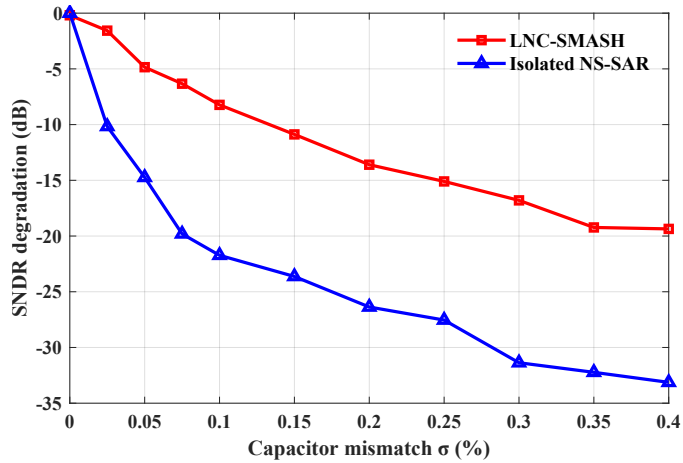


Fig. 6: Monte Carlo simulation of the SNDR degradation from the capacitor mismatch in the NS-SAR stage’s CDAC for the proposed LNC-SMASH vs the isolated NS-SAR second stage with 10kHz -3dBFS sine input.

the first stage DT  $\Delta\Sigma$ , the main sources of non-linearity in the proposed ADC arise from any capacitor mismatch in these circuit blocks. To study these non-ideal behaviors, as presented in Fig. 6, a first Monte Carlo simulation (50 iterations, 10kHz -3dBFS sine input) was realized to compare sensitivity to capacitor mismatch in the NS-SAR stage’s CDAC for the proposed architecture, as well as for the isolated NS-SAR. In a classical NS-SAR, CDAC errors do not get shaped and severely degrade SNDR. On the other hand, with the proposed SMASH architecture, NS-SAR’s CDAC errors get shaped by the DT  $\Delta\Sigma$  first stage and become less of a concern, removing the need for calibration.

A similar study was performed to compare the impact of capacitor mismatch within both stages’ SAR quantizers and main feedback DAC, as presented in Fig. 7. Contrary to the errors of the SAR quantizers, the error of the main feedback DAC does not get shaped. As such, the rapid deterioration of ideal SQNR relative to capacitor mismatch is striking, whereas SAR CDAC mismatch is not of concern, even when aiming for SNDR above 90 dB.

A simple first order element rotation “data weight averaging” (DWA) [15] was also tested in simulations to mitigate the deleterious effects of main DAC mismatch. Despite improved robustness, the SNDR still falls short of the 90 dB target. As such, calibration or higher order mismatch shaping would be necessary to achieve the desired SNDR. Nevertheless, the proposed architecture achieves a significant relaxation of the matching constraints of both SAR quantizers and NS-SAR FIR filter. High linearity requirements are now concentrated in one block: the main feedback DAC, which is a common issue for every  $\Delta\Sigma$  ADC. Further research should be pursued to elaborate new solutions to improve this critical block.

#### IV. CONCLUSION

In conclusion, this paper introduced the LNC-SMASH ADC architecture featuring a NS-SAR stage for the first time. The inclusion of NS-SAR allows for the cancelling of the first stage’s quantization noise, similarly to the MASH structure. Furthermore, the DT  $\Delta\Sigma$  implementation of the first stage shapes the signal-dependent error of the NS-SAR second stage, relaxing the matching and linearity constraints. System-level

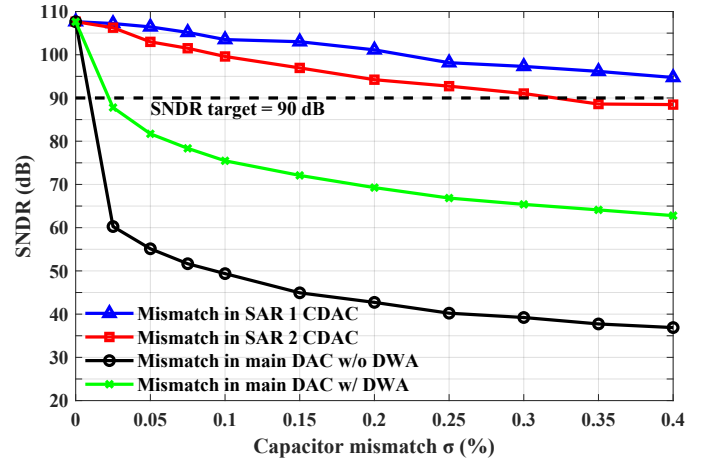


Fig. 7: Monte Carlo simulation of the SNDR of the proposed LNC-SMASH for different capacitor mismatch sources with 10kHz -3dBFS sine input.

simulations demonstrate a functional proof of concept and promising results for high precision, low-power applications.

#### REFERENCES

- [1] L. Jie, B. Zheng, H.-W. Chen, and M. P. Flynn, “A cascaded noise-shaping sar architecture for robust order extension,” *IEEE Journal of Solid-State Circuits*, vol. 55, no. 12, pp. 3236–3247, 2020.
- [2] J. A. Fredenburg and M. P. Flynn, “A 90-ms/s 11-mhz-bandwidth 62-db snr noise-shaping sar adc,” *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2898–2904, 2012.
- [3] L. Jie, X. Tang, J. Liu, L. Shen, S. Li, N. Sun, and M. P. Flynn, “An overview of noise-shaping sar adc: From fundamentals to the frontier,” *IEEE Open Journal of the Solid-State Circuits Society*, vol. 1, pp. 149–161, 2021.
- [4] G. M. Salgado, D. O’Hare, and I. O’Connell, “Recent advances and trends in noise shaping sar adcs,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 2, pp. 545–549, 2021.
- [5] S. Pavan, R. Schreier, and G. C. Temes, *Understanding delta-sigma data converters*. John Wiley & Sons, 2017.
- [6] T. Hayashi, Y. Inabe, K. Uchimura, and T. Kimura, “A multistage delta-sigma modulator without double integration loop,” in *1986 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, vol. XXIX, 1986, pp. 182–183.
- [7] M. Akbari, M. Honarparvar, Y. Savaria, and M. Sawan, “Ota-free mash 2–2 noise shaping sar adc: System and design considerations,” in *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2020, pp. 1–5.
- [8] S. Oh, Y. Oh, J. Lee, K. Kim, S. Lee, J. Kim, and H. Chae, “An 85 db dr 4 mhz bw pipelined noise-shaping sar adc with 1–2 mash structure,” *IEEE Journal of Solid-State Circuits*, vol. 56, no. 11, pp. 3424–3433, 2021.
- [9] N. Maghari, S. Kwon, and U.-K. Moon, “74 db snr multi-loop sturdy-mash delta-sigma modulator using 35 db open-loop opamp gain,” *IEEE Journal of Solid-State Circuits*, vol. 44, no. 8, pp. 2212–2221, 2009.
- [10] D.-Y. Yoon, S. Ho, and H.-S. Lee, “A continuous-time sturdy-mash delta-sigma modulator in 28 nm cmos,” *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 2880–2890, 2015.
- [11] C. Han and N. Maghari, “Delay based noise cancelling sturdy mash delta-sigma modulator,” *Electronics letters*, vol. 50, no. 5, pp. 351–353, 2014.
- [12] J. Ungethüm, M. Pietzko, J. G. Kauffman, Q. Li, and M. Ortman, “Maximizing the inter-stage gain in ct 0-x mash delta-sigma-modulators,” in *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2022, pp. 561–565.
- [13] R. Schreier. (2023) Delta sigma toolbox. MATLAB File Exchange. [Online]. Available: <https://www.mathworks.com/matlabcentral/fileexchange/19-delta-sigma-toolbox>
- [14] X. Tang, X. Yang, W. Zhao, C.-K. Hsu, J. Liu, L. Shen, A. Mukherjee, W. Shi, D. Z. Pan, and N. Sun, “9.5 a 13.5b-enob second-order noise-shaping sar with pvt-robust closed-loop dynamic amplifier,” in *2020 IEEE International Solid-State Circuits Conference - (ISSCC)*, 2020, pp. 162–164.
- [15] R. Baird and T. Fiez, “Improved delta-sigma dac linearity using data weighted averaging,” in *Proceedings of ISCAS’95 - International Symposium on Circuits and Systems*, vol. 1, 1995, pp. 13–16 vol.1.