A Rail-to-Rail Low-Power Dynamic CMOS Amplifier for Switched-Capacitor Filters in High-Performance ADC

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***Abstract*—This paper presents a novel rail-to-rail low power dynamic CMOS amplifier optimized for discrete-time filtering in analog-to-digital converters (ADC). The proposed architecture incorporates a switched resistor-capacitor (RC) parallel compensation technique, which is strategically activated in the sampling phase to minimize the amplifier's current consumption. Dynamic biasing of the amplifier further improves energy efficiency by slashing high slewing currents once linear settling takes over. Simulation results in 65 nm CMOS exhibit 3.2 times reduction in power consumption with respect to a comparable static amplifier. Accurate integration waveforms are achieved while consuming a mere 239 μW for 6 τ settling under 4.9 ns.**

***Index Terms*—dynamic amplifier, rail-to-rail, low power, switched-capacitor integrator, loop filter, ADC, delta-sigma**

I. Introduction

With the ever shrinking transistor sizes in deep submicron technology nodes, analog designs are more challenging than ever. Indeed, the reduced supply voltages impose significant circuit constraints as the exploitable headroom is compressed. To make things worse, system specifications are also increasingly demanding. In portable, battery powered, embedded applications like sensor nodes or edge AI, every microjoule of energy must be squeezed to optimize autonomy and battery size. At the same time, such systems integrate complex analog building blocks, mainly high-performance analog-to-digital converters (ADC) to interface with sensors. These blocks typically require amplifiers to process analog signals, which tend to be among the most power-hungry circuits [1].

To meet these ever-tightening design constraints, state-of-the-art data converters propose many ingenious strategies for lowering power consumption while improving performance. One interesting solution dating back to the late 70s is the dynamic amplifier [2], [3]. Contrary to a standard amplifier with static biasing, the biasing current of a dynamic amplifier is not constant, but rather varies during the amplification phase. Dynamic amplifiers are intended for discrete-time signal processing applications as their output varies with time and requires a periodic cycle to be processed, which is a perfect match for discrete-time ADC based on switched capacitors (SC). The ability to vary the biasing current of the amplifier during its operating cycle allows for better balancing of power usage.

Dynamic amplifiers come in a plethora of topologies. Some make the bias current input dependent [4], while others refine the more classical design of a discharging capacitor inside a differential pair gain stage [5], [6]. Polyphase amplifiers switch resistors during operation to adjust amplifier properties [7], [8]. Other innovative dynamic amplifier topologies have been proposed such as the floating inverter amplifier, first presented as a StrongARM latch preamplifier [9], and then in noise-shaping SAR as the loop filter [10].

The driving principle of these topologies is to make the amplifier properties vary with time in order to reach a better tradeoff between power consumption, amplifier response, settling time and noise. However, they usually rely on discharging a capacitor, which reduces output swing and limits settling speed.

This work proposes a different approach to the dynamic amplifier based on a 2-stages amplifier with a rail-to-rail, class AB output stage with high drive capability. The design is intended to serve as the amplifier inside a switched-capacitor integrator, meant to be used as loop filter in a discrete-time $\Delta\Sigma$ ADC. The operation of the dynamic amplifier takes place in two parts. Firstly, the compensation of the amplifier is dynamically adjusted to always satisfy phase margin while simultaneously keeping capacitive loading at a minimum. Secondly, the bias current of the input stage is dynamically controlled with a switched-ratio dynamic current mirror, allowing the biasing current to be reduced as the amplifying phase progresses. This approach allows ample current for fast slewing, while preserving low power consumption when linear settling occurs further down the settling phase.

This paper is organized in three sections. First, section II covers the proposed rail-to-rail dynamic amplifier topology. Next, section III presents a SC integrator design within a $\Delta\Sigma$ ADC with simulation results. Finally, a conclusion wraps up the article.

II. Proposed Amplifier Topology

A. Design Overview

The target application of the dynamic amplifier is as a fully differential amplifier inside a SC integrator circuit (inspired from [11]) as shown in Fig. 1. This circuit is a typical loop

filter in discrete-time $\Delta\Sigma$ ADC and is the proposed use case of the novel dynamic amplifier topology. The amplifier is specifically tailored to be working in this topology for reasons that will become evident soon.

The proposed dynamic rail-to-rail amplifier is presented in Fig. 2. The main idea is to form a differential pair as the first stage, coupled with a rail-to-rail Class AB second stage, featuring time-varying biasing and stability compensation. The amplifier compensation can be turned off during the main amplification phase of the SC circuit (ϕ_2 in Fig. 1) so as to greatly reduce capacitive loading and hence current requirements of the first stage. Varying the bias current of the same differential pair allows for further reduction of power consumption by yielding a more efficient bias point after the slewing phase during settling. Moreover, the resistive common-mode feedback (CMFB) shifts the bias point of the output stage as the current varies, allowing optimization of the power consumption of both stages only by controlling one current source. High amplification gain is achieved through the cascade of the two stages. Each part of the circuit is explained in more detail below.

B. First Stage

The first stage is a fully differential pair with active load. The input NMOS ($M_{1,2}$) are biased in subthreshold to achieve high transconductance, hence high gain, efficiently. The active load PMOS ($M_{3,4}$) are in moderate inversion so that their transconductance is just below that of $M_{1,2}$ to reduce thermal noise, as will be explained in a following subsection.

The biasing of the first stage is ensured by a variable current source. The core concept behind varying the bias current of the amplifier is its operation in a discrete-time, settling-based context, where the input arrives in steps from the previous discrete sample. Convergence toward the settling point occurs in two phases: a slewing phase, followed by a linear settling phase. Both phases require different bias currents, slewing being generally the most power hungry. One can ensure fast slewing by providing sufficient biasing current during that phase, while decreasing biasing current as much as possible during the linear settling phase to save on power.

The CMFB of this first stage consists of two buffers with two resistors, enabling fast common-mode extraction without loading the stage nor reducing its gain. Fast CMFB is necessary to accurately track the common-mode changes as the bias current varies during amplification. This common-mode scheme allows the adjustment of the common mode in response to current variations. Specifically, reducing the bias current in the differential pair during amplification decreases the overdrive voltage of the active load PMOS ($M_{3,4}$), consequently increasing the output common-mode DC voltage through the CMFB. The rising common mode at the output of the first stage changes the biasing of the second stage, enabling it to achieve the same power savings as the first stage.

The optimal biasing current was determined considering high-level simulation settling performance and design complexity. To maintain the design as simple as possible while ensuring good performance, an exponential current waveform

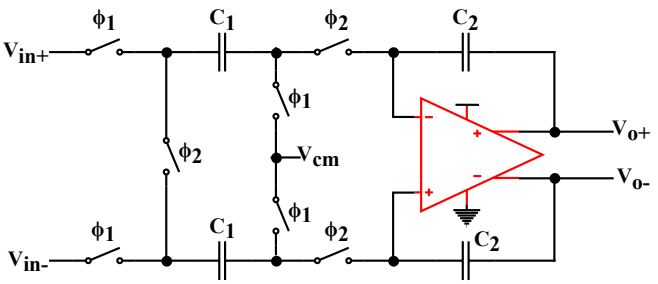

Fig. 1: Schematic of the switched-capacitor integrator targeted by the amplifier design.

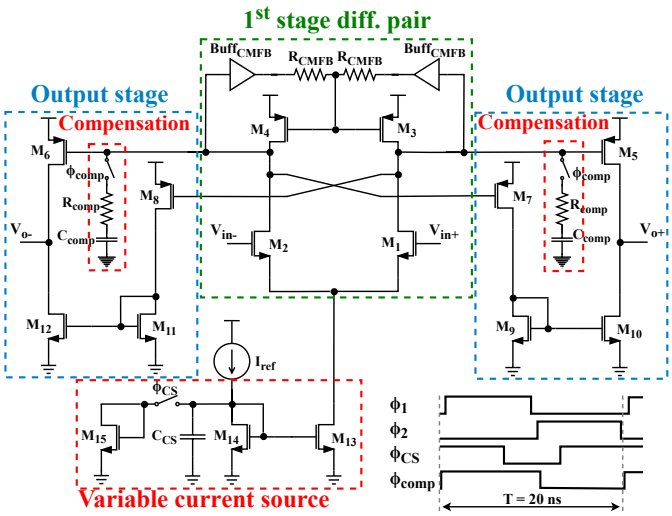

Fig. 2: Schematic and clock diagram of the proposed low-power rail-to-rail dynamic amplifier. The common-mode feedback of the output stage is omitted for clarity.

was selected. Although switching the current in a stepwise manner is easier to implement (saving capacitor C_{CS}), sharp current transitions may cause undesirable swings in the DC operating point of the amplifier. The waveform of the biasing current and the output common mode of the first stage are presented in Fig. 3 to better illustrate the concept.

C. Variable Current Source

The variable current source consists of $M_{13\text{-}15}$, switch ϕ_{CS}, capacitor C_{CS} and a copy of the reference current source of the IC, represented by the DC source I_{ref} in Fig. 2. The objective is to reliably generate an exponentially descending current between two DC values. A process-voltage-temperature (PVT) robust method for achieving a step change in current involves the use of a current mirror with a varying ratio. The current is determined by I_{ref} times the size ratio M_{13}/M_{14} for the high current at the beginning of the amplifying phase when ϕ_{CS} is open. Afterwards, as ϕ_{CS} closes, the current shifts towards I_{ref} times the size ratio $M_{13}/(M_{14}+M_{15})$, shifting the current to a lower value. The transition between the initial and final current values is smoothed by capacitor C_{CS} to emulate an exponential curve. Mathematically deriving the waveform for ideal MOSFET and switches results in a hyperbolic tangent current waveform, which can be closely approximated to the

desired exponential curve in Fig. 3 through precise device sizing.

D. Output Stage

The output stage is a class AB output stage inspired from [12]. It consists of PMOS $M_{5,6}$ in a common-source amplifying stage, with a current mirror drawing input from the opposite polarity branch as its source of biasing. Through this arrangement, the biasing current of the stage is increased in the event of a large swing input: as one of the differential output nodes of the first stage is pulled down, the bias current through the mirror rises, thereby enhancing drive capability and limiting slewing.

The varying common mode at the input of $M_{5,6}$, which follows the variable bias current of the first stage, also allows for the biasing of this stage to be varied by adjusting the level of the biasing output mirrors, as illustrated in Fig. 3. Consequently, both stages can benefit from higher current for slewing at the beginning of the amplification phase, and lower current during linearly settling towards the end of the phase.

The CMFB of this stage (not depicted in Fig. 2), is achieved through resistive sensing, followed by an error amplifier with a reference voltage fixed at the desired common mode. This amplifier then acts on the gates of two additional NMOS transistors in parallel with M_{10} and M_{12} to adjust the current necessary to maintain an accurate common mode at half the supply voltage, ensuring rail-to-rail swing.

E. Stability and Switching Compensation

To minimize power consumption, the dominant pole is strategically placed at the output of the amplifier, where large switched capacitors are located due to the integrator topology in which the amplifier is inserted, avoiding the need for an additional dominant Miller compensation. Furthermore, simulations have demonstrated that the combination of large switched capacitors and switch resistance introduces a zero in the frequency domain, providing adequate phase margin to ensure stability during the amplification phase as shown in Fig. 4. However, once the amplification phase ends and switches are closed, this zero vanishes as the switched-off resistance becomes too large, and the phase margin drops to a dangerously low level. Consequently, a RC compensation network is activated with ϕ_{comp} during the sampling phase and deactivated as soon as the amplification phase begins. This approach allows the amplifier to maintain a sufficient phase margin throughout its operation while avoiding capacitive loading during the amplification phase. As such, this approach reduces the current requirement for the first stage differential pair. Transient waveform disruption caused by the additional circuit switching is minimal and occurs at the beginning of the phase, ensuring that no significant error remains once convergence is achieved.

F. Noise Considerations

The thermal noise of a SC integrator as the one targeted in this work is derived in [11] for a conventional differential pair amplifier. The assumption remains valid for the proposed topology since the first stage is still a differential pair, and the

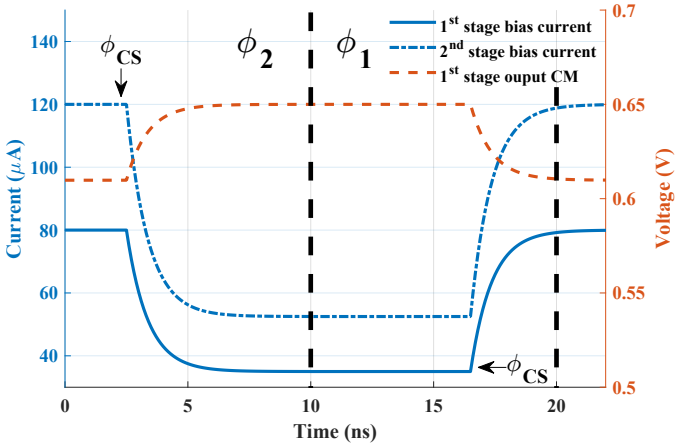

Fig. 3: Ideal waveform of the biasing current during amplification (ϕ_2) and sampling (ϕ_1) phases, highlighting the change in common mode voltage between the two stages caused by current variation in the first stage.

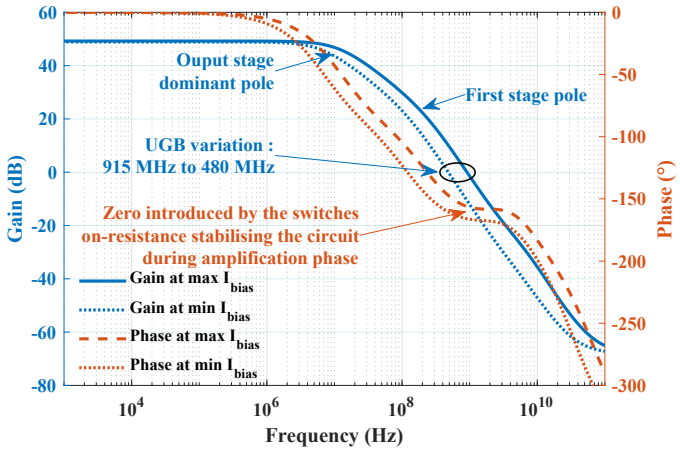

Fig. 4: Simulation results of the AC response of the proposed amplifier during the amplification phase for the highest and the lowest varying bias current.

input-referred noise of the second stage is reduced by the gain of the first stage, rendering it negligible. The total noise for both phases is thus

$$\overline{v_n^2} = \left(\frac{2kT}{C_1}\right)\left(2 + \frac{\gamma_{amp} - 1}{1 + g_m R}\right), \tag{1}$$

with

$$\gamma_{amp} = \gamma\left(1 + \frac{g_{m3}}{g_{m1}}\right), \tag{2}$$

where γ is a device-dependent fitting parameter with a theoretical value of 2/3, k the Boltzmann constant, T the absolute temperature in kelvin, g_m the transconductance of the differential pair, R the resistance of the switch and g_{m1} and g_{m3} respectively the transconductance of M_1 and M_3. Therefore, to ensure low noise, g_{m3} should be considerably lower than g_{m1}. Biasing the input NMOS in subthreshold guarantees the highest g_{m1} for a given current. As the NMOS is in the same differential pair as the PMOS, it carries the same biasing current and it is therefore sufficient to bias M_3 in moderate

inversion to obtain $\gamma_{amp} \approx 1$. The input-referred noise then reduces to

$$\overline{v_n^2} = \frac{4kT}{C_1}. \quad (3)$$

III. Example Design in CMOS 65 nm

A. Design

The proposed rail-to-rail low power dynamic amplifier was initially developed for use in a SC integrator for a $\Delta\Sigma$ ADC. The targeted ADC is a 2+2 LNC-SMASH with a noise-shaping SAR second stage [13]. An amplifier design that meets requirements for the first integrator of the SC loop filter will be presented here. The design is realized using the TSMC 65 nm PDK at 1 V supply.

The target SNR is 90 dB, while the design is thermal noise limited as the SQNR is in excess of 100 dB with an oversampling ratio of 20. The sampling frequency is 20 MS/s, with 10 ns allowed for the amplifying phase and another 10 ns for the sampling phase (the rest of the time is allowed for the second stage noise-shaping SAR).

Maintaining a 3 dB margin, the thermal noise limit is given by

$$\overline{v_n^2} = \frac{V_p^2/2}{10^{\frac{SNR}{10}}}, \quad (4)$$

which yields (11 μV)^2. Using (3), the minimum required capacitor is computed to be 6.8 pF. Dynamic range scaling is added as high-level simulation conducted in [13] indicates an output swing of 80 mV. Rail-to-rail functionality of the amplifier is highly beneficial as dynamic range scaling allows for significant reduction of the feedback capacitors and total output noise. Full swing of 1 V allows for a dynamic range scaling of 8, yielding C_2 of 0.85 pF.

Gain requirements are declined in 2 criteria. Finite gain will result in errors in the transfer function of the modulator and in dead zone preventing small input resolution. Both criteria are explained in [11] and are expressed as the following:

$$A > \frac{OSR}{\pi}\frac{C_1}{C_2} - 1, \quad (5)$$

$$A > \sqrt{\frac{p}{\delta}}, \quad (6)$$

where OSR is the oversampling ratio, p the amplitude of the recurring pattern when the input is grounded (determined by high-level simulation) and δ the dead zone. The design aims to ensure a dead zone smaller than 10 μV and 3 dB SQNR loss, resulting in a minimum gain requirement of 43 dB. This requirement aligns with previous analysis of 2-stages SMASH $\Delta\Sigma$ ADC [14].

The variable current needed form the variable source has been determined in simulation to yield the required 10 ns settling with as low total power consumption as possible.

B. Simulation Results and Comparison with Static Amplifier

Fig. 5 shows the step response of the proposed amplifier in comparison with an equivalent statically-biased amplifier and the same statically-biased amplifier with a static compensation. Although all responses are nearly identical, the fully static amplifier needs a 460 μA bias current for satisfactory slewing in the first stage. Removing compensation during the amplification phase allows an impressive bias current reduction to 70 μA while keeping the same slewing as no compensation capacitor slows down the amplifier. Finally, the proposed amplifier with the switched compensation and the dynamic bias current allows for variation from 80 μA to 35 μA and from 120 μA to 60 μA for the first and second stage bias current respectively. Table I summarize the comparison of the proposed amplifier with the equivalent static designs. The proposed switched compensation allows 2.6 times power consumption reduction while the dynamic biasing further reduces power consumption by 20% for the same 6 τ settling time of 4.9 ns. All amplifiers exhibit a sufficient DC gain of 50 dB meeting all requirements with a comfortable margin for parasitics and process variations in a forthcoming fabricated prototype.

Fig. 6 shows the ramp response of the SC integrator presented in Fig. 1 incorporating the proposed dynamic amplifier. The transient response shows excellent tracking of the ideal output when taking into account the finite 50 dB gain of the amplifier, which necessarily causes leakage in the SC since the input can't be at perfect virtual ground and C_1 loses charges due to the non-zero input voltage [15]. The rail-to-rail output stage is shown in action, where error only starts to manifest

TABLE I: Comparison of the proposed dynamic amplifier with equivalent static amplifier designs

Design	Proposed	Static bias current	Static bias current and compensation
Open-loop DC gain (dB)	**48.9-49.3**	49.3	49.1
6 τ settling time (ns)	**4.9**	4.9	4.9
Power consumption (μW)	**239**	287	770

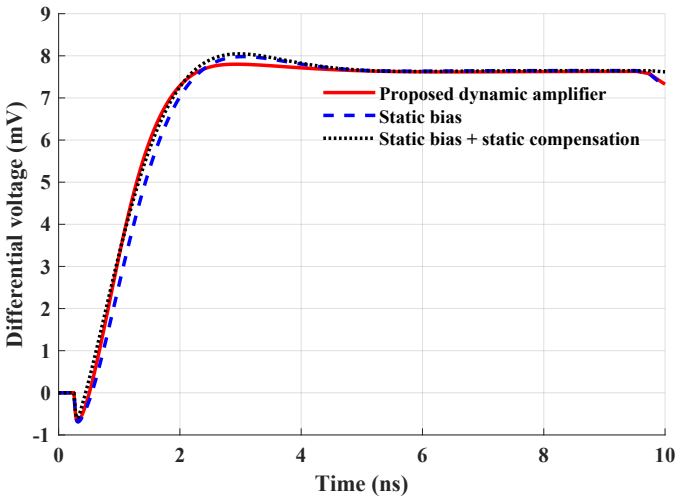

Fig. 5: Step response comparison between the proposed dynamic amplifier and an equivalent static-current and static-compensation amplifier during the amplification phase. The response is similar, yet the proposed amplifier cut the power consumption in more than half in comparison with the static compensation case and further improves by 20% from the static bias case.

significantly at 925 mV swing due to the output transistors starting to exit the saturation region. As such, the maximum integrator output is determined to be 975 mV swing.

IV. Conclusion

To conclude, this work introduced a novel rail-to-rail low power dynamic amplifier that is exceptionally well-suited for performing discrete-time filtering in high-precision oversampling ADC. The proposed design leverages a switched compensation scheme to minimize capacitive loading and employs a dynamic biasing scheme to limit power consumption while maintaining fast settling speed. Simulations show a power reduction by 3.2 times compared to a comparable static biasing amplifier, along with accurate integration across more than 90% of the entire rail-to-rail swing.

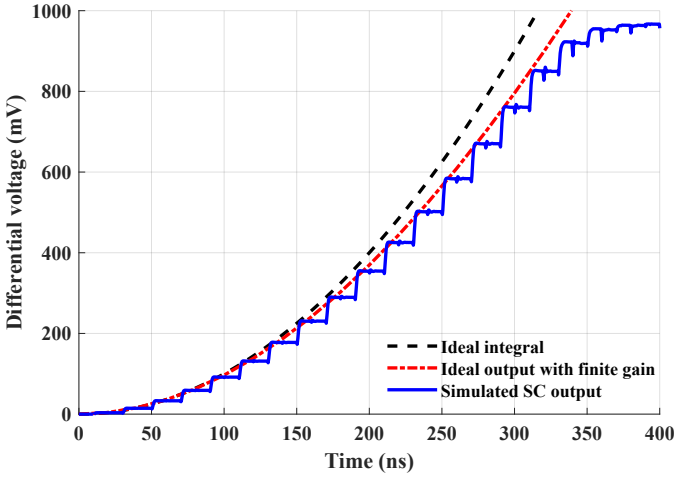

Fig. 6: Ramp input transient response of the SC integrator incorporating the proposed dynamic amplifier. The maximum output swing reaches 975 mV on a 1 V supply.

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